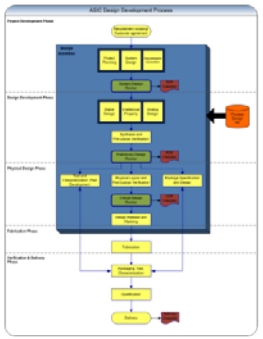
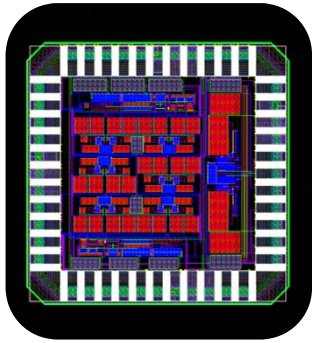
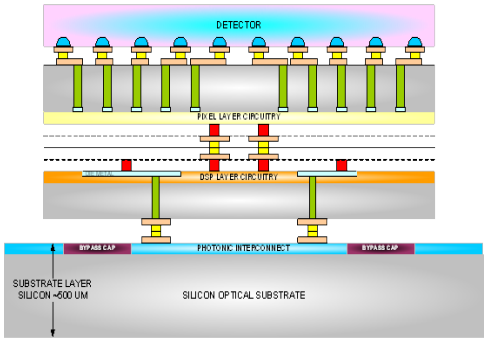
Exceptional service in the national interest

Sandia National Laboratories







HPC Computing & SoC Design @ Sandia National Laboratories

Design Automation for HPC, Clouds, & Server-Class SoCs

Workshop 6, DAC 2015

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June 7, 2015

U.S. DEPARTMENT OF ENERGY | NNSA National Nuclear Security Administration

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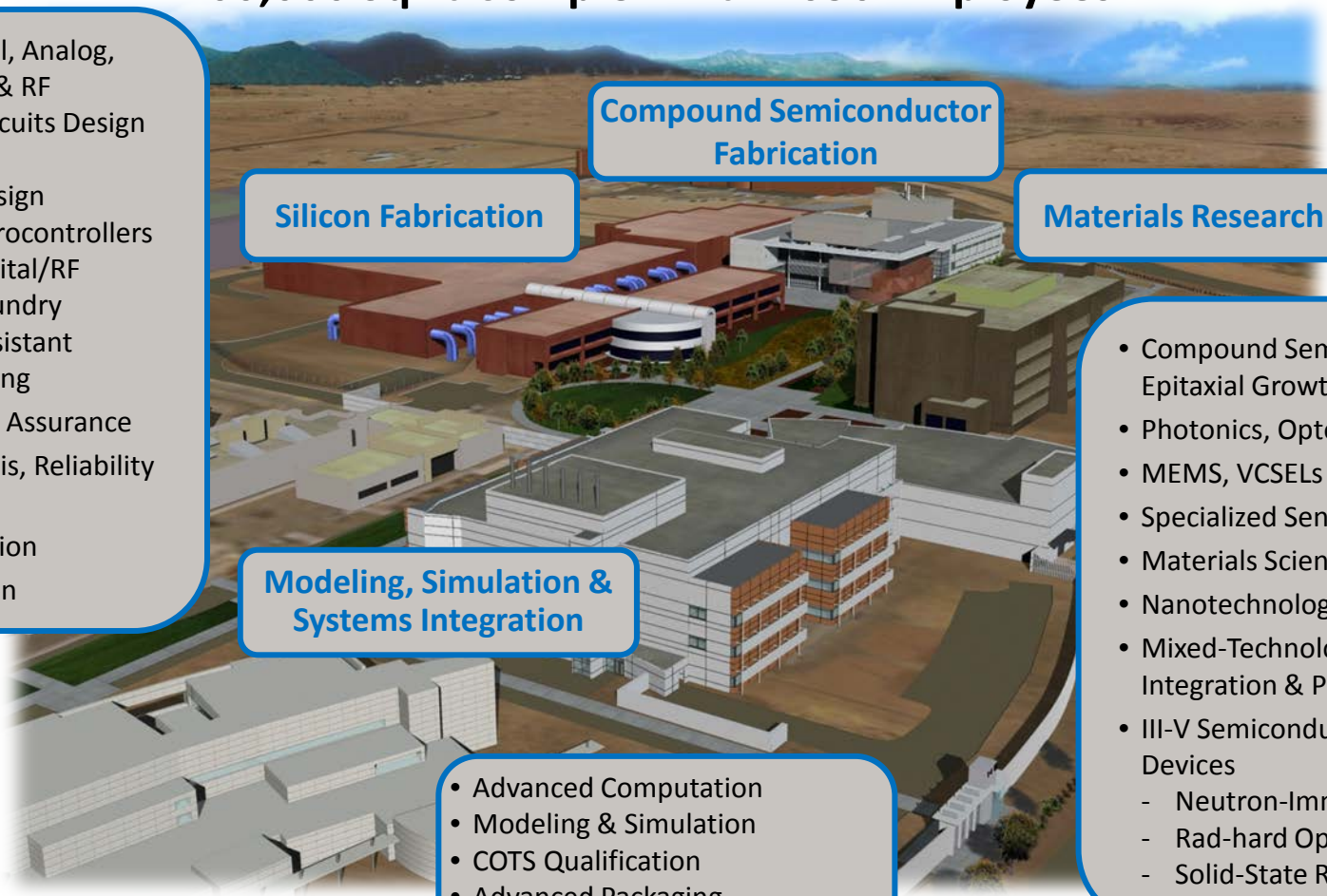
Sandia Microsystems & Engineering Sciences Applications (MESA)

Sandia National Laboratories

400,000 Sq-ft Complex with >650 Employees

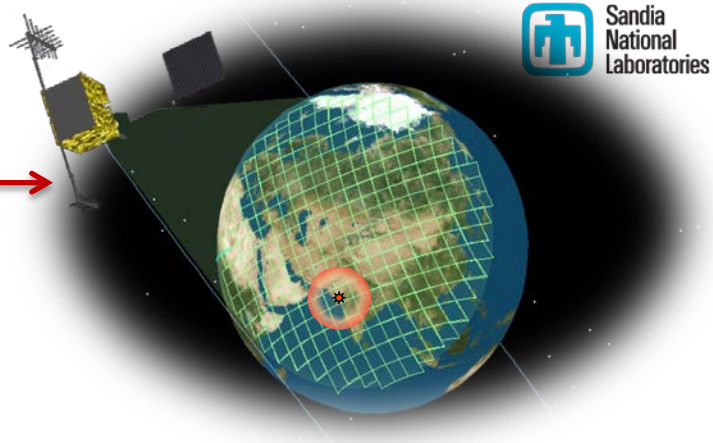
- Trusted Digital, Analog, Mixed Signal & RF Integrated Circuits Design & Fabrication
- Custom IC Design
  - Secure microcontrollers
  - Analog/Digital/RF
  - Trusted Foundry
  - Tamper Resistant
- Micromachining
- RAD Effects & Assurance
- Failure Analysis, Reliability Physics
- Test & Validation
- 3-D Integration



- Advanced Computation
- Modeling & Simulation
- COTS Qualification
- Advanced Packaging
- Custom Electronic Components
- System Design & Test

- Compound Semiconductor Epitaxial Growth
- Photonics, Optoelectronics
- MEMS, VCSELs
- Specialized Sensors
- Materials Science
- Nanotechnology, Chem/Bio
- Mixed-Technology Integration & Processing
- III-V Semiconductor Devices
  - Neutron-Immune HBT
  - Rad-hard Optical Links
  - Solid-State RF Devices

HPC/SoC Applications At Sandia



- Remote Sensing
- Traditional Modeling & Simulation Applications
- Biological & Chemical Sensors
- Synthetic Aperture Radar (SAR)

- In-Situ Data Analysis In Harsh Environments
- Autonomous Operation

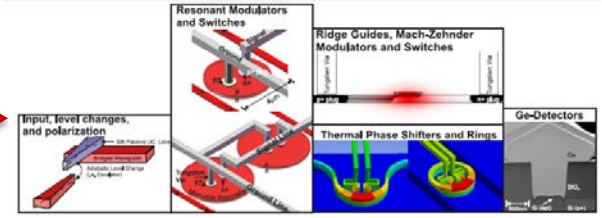
- Engineering & Sciences Applications

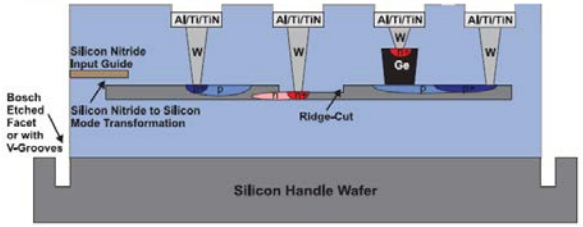
Many non-traditional HPC applications at Sandia are focused on “Smart Sensors” that require embedded high performance analytic and data reduction capability.

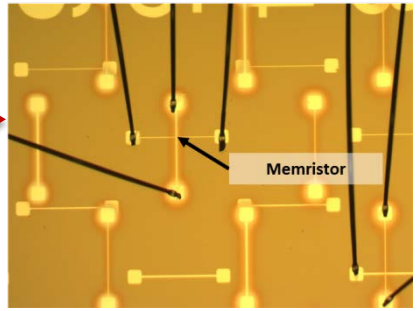
HPC Related Research At Sandia

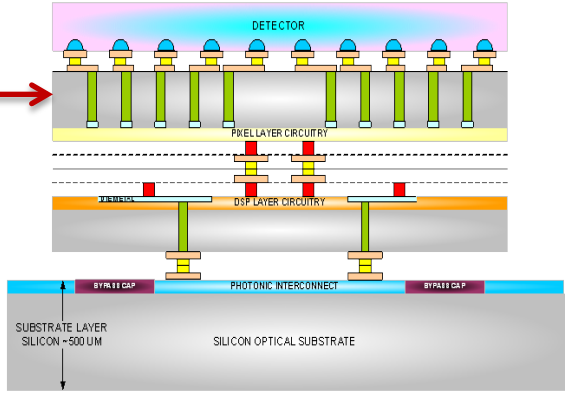
Sandia National Laboratories

- Silicon Photonics
- High Performance Computing (HPC) Architectures
- Beyond Moore Computing (BMC)
- Advanced Memories
- Neuro Inspired Algorithms
- 3D/Heterogeneous Integration
- Performance Measurement Units
- System Software Development





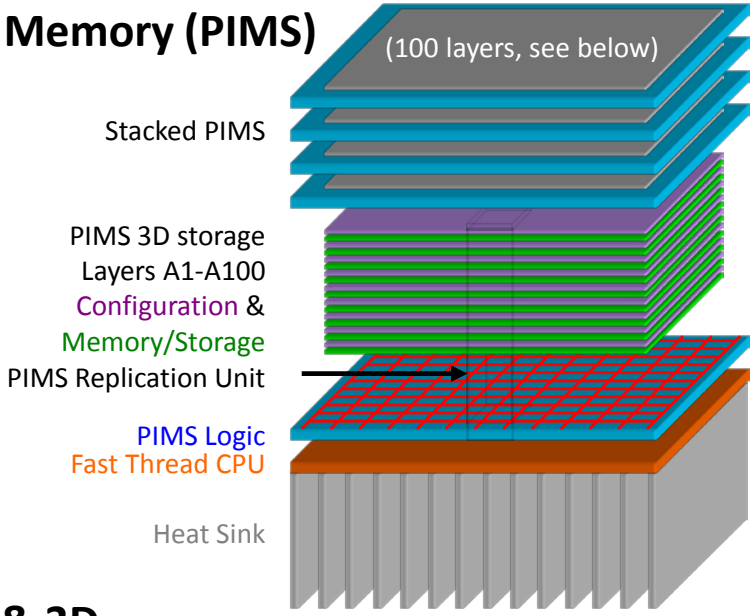




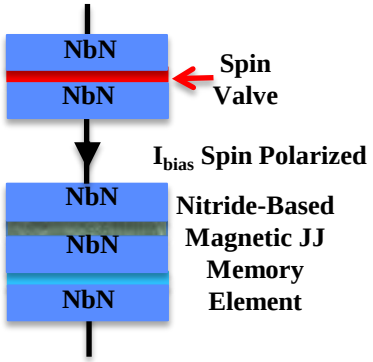
Current HPC Related Research At Sandia

Sandia National Laboratories

- **Processing-In-Memory-and-Storage Using Advanced Memory (PIMS)**
  - Physical Implementation
    - Base layer ➔ PIMS Logic & Advanced Memory
  - Target Applications
    - Scientific
    - Neuromorphic
    - Data Analytics



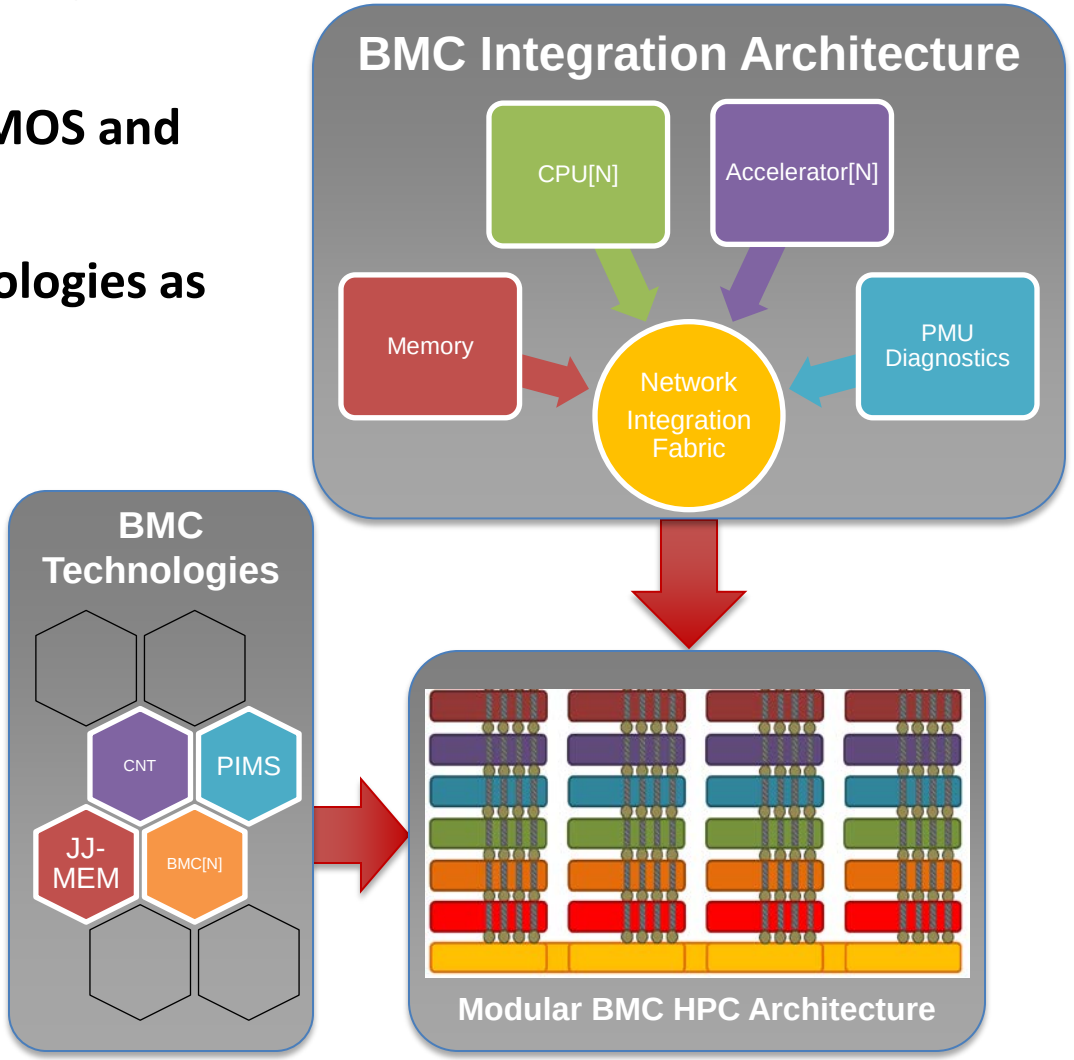
- **Niobium Nitride-Based Josephson Junction Memory & 3D Integration for Scalable, Low-Power, High Performance Computing**
  - Superconducting electronics has the potential to decrease power consumption relative to end of roadmap CMOS by 100x while still maintaining high performance.
  - Nitrides have higher temperature stability than standard Nb-based process providing potential for 3D scaling.
  - Nitride JJ has potential for higher yield relative to Nb/Al-AlOx/Nb.



Proposed Beyond Moore Computing Modular R&D Architecture

Sandia National Laboratories

- **Platform to support incremental integration of BMC technologies**
- **Can be implemented in today's CMOS and augmented with BMC**
- **Flexibility to integrate BMC technologies as they are developed**
- **Scalable architecture**
- **PMU diagnostics enable…**
  - Dynamic adaptive runtime system software capability.
  - Measurement of data movement and energy consumption for caches buses and memory.
- **Network / architecture to achieve maximum flexibility?**



3D & Heterogeneous Integration @ Sandia

Sandia National Laboratories

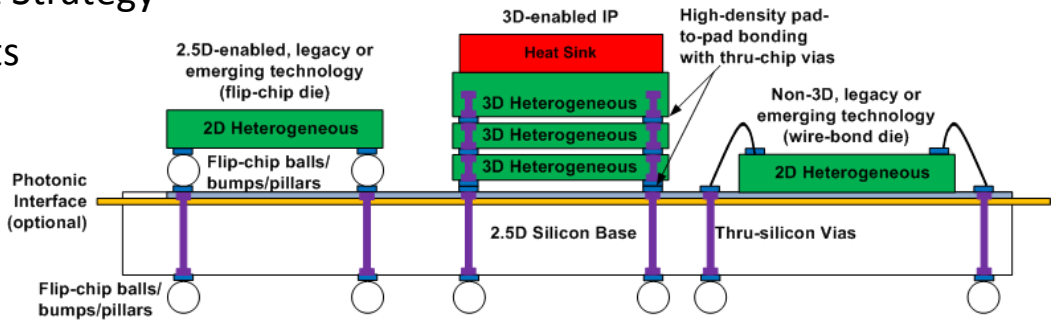
- **Technologies**
  - Indium Bump
  - Oxide-Oxide Bond
- **Low Volume, High Reliability**
- **Custom Platforms (R&D & Production)**
- **Heterogeneous Integration (III-V, Etc.)**
  - III-V (GaAs, InP, Etc.)
- **Heterogeneous CMOS Post Processing**
  - Resistive Memory (Memristors)
  - Aluminum Nitride (AlN) Resonator
- **Applications**
  - Image Sensor Hybridization (dual layer)
  - Multi-layer (4+) 3D microsystems & sensors
  - High Performance Computing
    - BMC Modular Architecture
    - Stack-N-Pack (CPU-Memory-CPU)

	Indium Bump	Oxide Bond
Density	Moderate	High
Minimum Pitch	10-15µm	<10µm
Method	D2D, D2W	W2W
Underfill?	Yes	No
Maturity @SNL	Moderate	In Development

W2W = Wafer To Wafer Bonding
D2W = Die To Wafer Bonding
D2D = Die To Die Bonding

HPC R&D 3D Integration Considerations

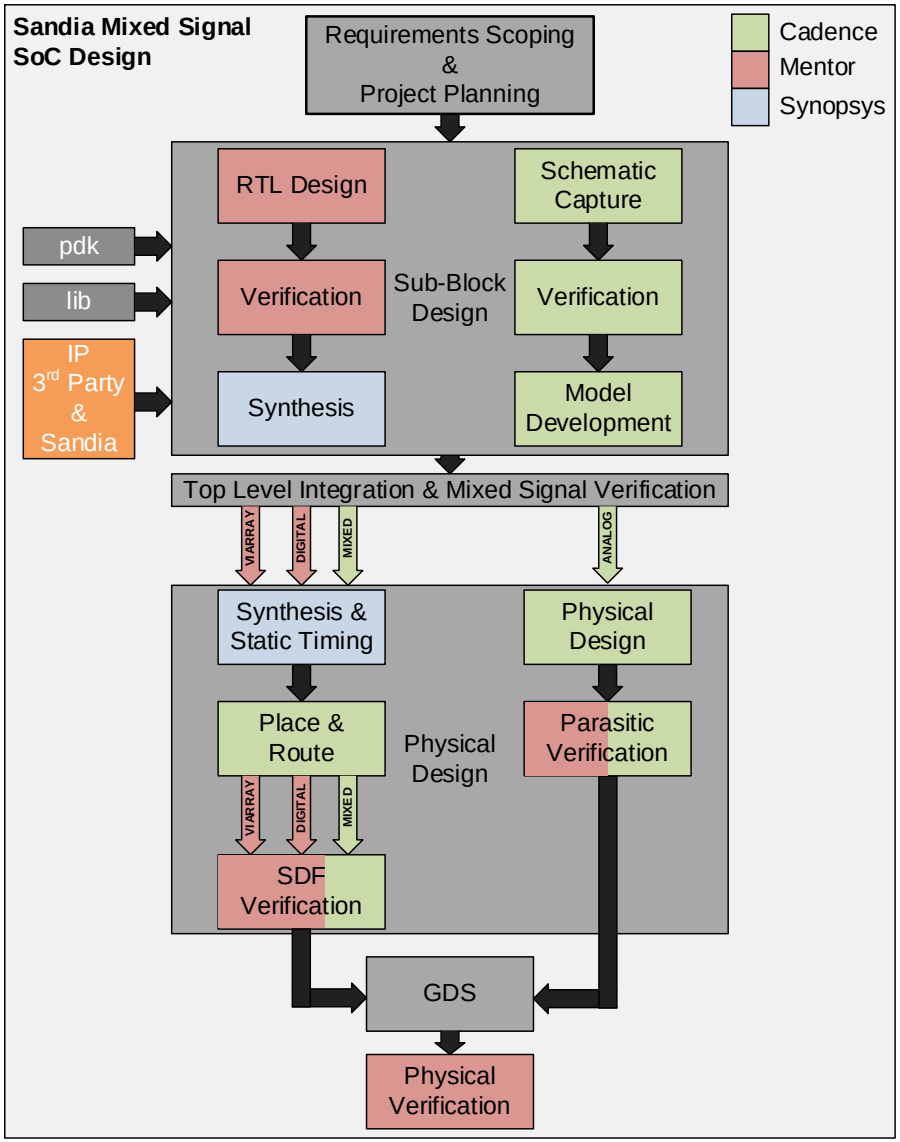
- Circuit/Function Partitioning & Placement Strategy
  - Performance & Density Requirements
  - Power/Thermal Dissipation
  - Yield & Test
- Testing & Failure Analysis Strategy
  - BIST, ATPG, JTAG, Etc.
  - Wafer Probe, Known-Good-Die/Stack, Wafer Mapping, Etc.



- Thermal Modeling (Thermo-Electrical & Thermo-Mechanical) & Packaging
- Layer-to-Layer Interconnect Density
  - Through-Silicon-Via (TSV) & Face-To-Face Bond Requirements (diameter, pitch)
  - Stacked Alignment Accuracy
- Wafer Level vs. Die Level Requirements Assembly & Cost
  - Most High Density Processes Require Wafer-To-Wafer Bonding
    - Wafer level processing required to define TSV's and interconnect layers
    - Wafer level processing required to thin wafer backside to reveal TSV's
  - Wafer Level Fabrication At Advanced Technology Nodes Can Be Cost Prohibitive For R&D
  - Costs Are More Manageable Using Multi-Project Wafer (MPW) Runs
    - Wafer contains designs for other users; Often only die are ultimately available, which can complicate 3D processing approach
    - Circuitry must be partitioned to contain interconnect density

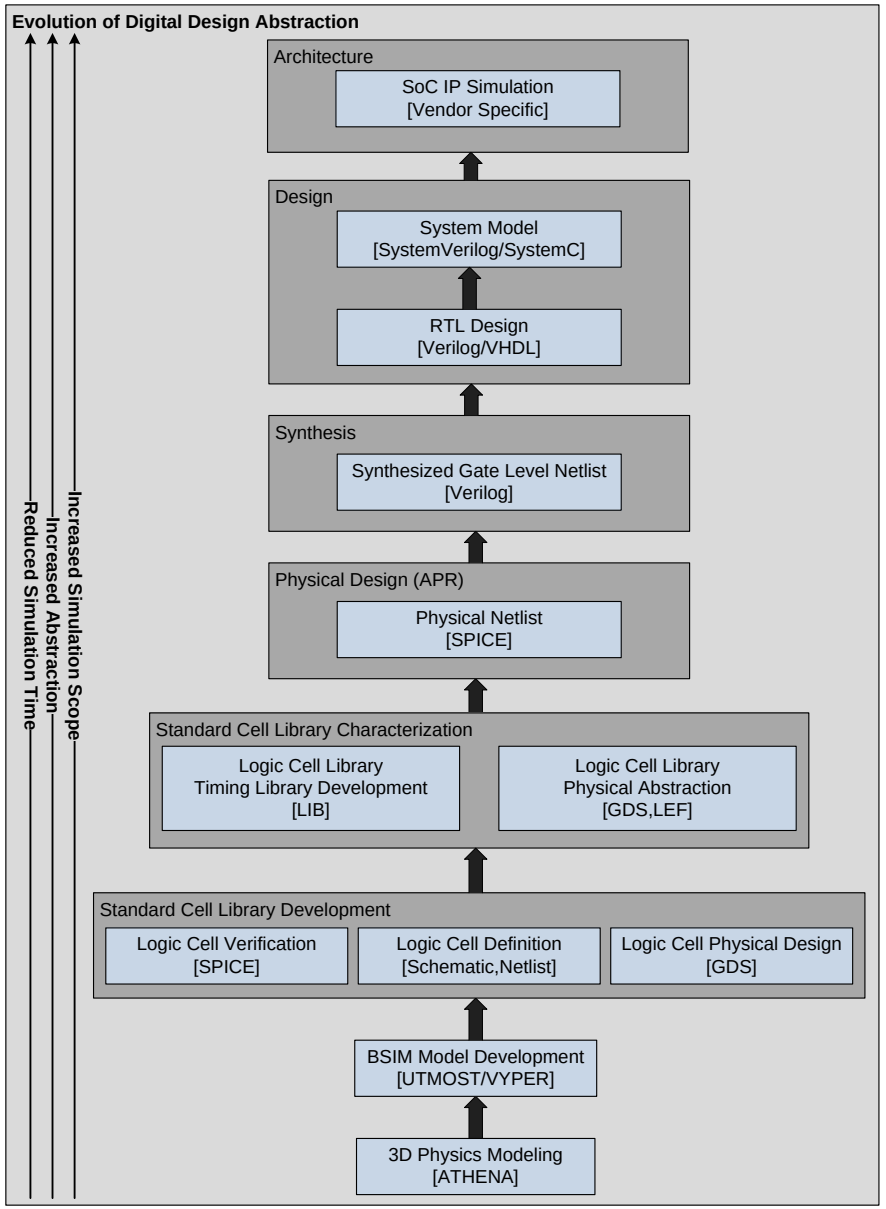
Sandia Mixed Signal SoC Design

- Full Mixed-Signal IC Design Flow
  - Industry Standard EDA/CAD Tools
  - Mixed-Signal Verification & Co-Simulation
    - SPICE; Verilog-A; AMS; RTL
- SoC Verification
  - Universal Verification (UVM)
  - Formal Verification
- Synthesis & APR Flow
- Intellectual Property (IP)
  - Silicon Fabric/Motherboard SoC Design
  - Integration & Verification
  - Custom IP (Hard & Soft)
- 3D Integration & Verification Flow
  - 3D Automated Place & Route
  - 3D Verification



SoC Design Abstraction Evolution & HPC

- Evolution of abstraction (CMOS)
  - Driven by complexity, cost, & time to market
  - Analogous to the evolution of COTs PCB design
  - Chip scale architecture evaluation & trade space
  - Rapidly optimize architecture to the problem
- New hierarchy of designers in SoC development
  - System level designers drive architecture trades
  - Enabled by rapid prototyping & simulation tools
  - Drives high performance scalable platforms
- Proliferation of suite of IP building blocks
  - Silicon fabric or motherboard (3D?)
  - Reduced cost and risk
    - Pre-verified IP with design kits
    - Verification suite
    - Optimized for yield and manufacturing
- How do we enable/evolve abstraction for BMC technologies?



Comments On HPC R&D Rapid Prototyping & EDA

Sandia National Laboratories

- Development of new advanced verification techniques, increased abstraction, and expanded capacity will support larger verification scope and hardware-software co-design.
- How do we facilitate integration of BMC technologies?
  - Technologies can't be abstracted same way as CMOS (i.e. super-conducting logic).
  - How readily can these technologies be incorporated into existing EDA?
- Tighter EDA integration for 3D IC capabilities and standards will be required.
  - 3D Aware Routing
  - 3D Layout Vs. Schematic (LVS)
  - Floorplanning & Architecture Exploration (Partitioning)
  - Thermal aware design tools (Thermo-Electrical & Thermo-Mechanical)
  - Manufacturing defect detection (BIST, ATPG, DFT). Currently there are many techniques but not all are automated or integrated with industry standard CAD tools.
- Access to low cost, low volume, 3D integration technologies will facilitate R&D and heterogeneous BMC technology integration.
- Development of 3D failure analysis techniques will be required to improve yield and understand defects.