Design Automation for HPC, Clouds, and Server-Class SoCs

DAC2015 Workshop (June 07, 8:30am – 5:00pm | Room 304, Moscone Center)

Agenda

- 08:30 – 09:00 Intro/Greetings
- 09:00 – 09:30 Welcome and Overview
    - John and Jim & DARPA, DOE, DOD, NSF statements
- 09:30 – 10:00 Keynote Address
    - Shekar Borkar – Intel
- 10:00 – 12:00 System Integrators
    - 10:00 – 10:20 ARM (Rob Aitken)
    - 10:20 – 10:40 Break
    - 10:45 – 11:05 Sandia (Mike Holmes)
    - 11:10 – 11:30 ACS (Noel Wheeler)
    - 11:35 – 11:55 DARPA (Linton Salmon)
- 12:00 – 13:00 Lunch
- 13:00 – 14:00 Discussion Topic 1: Requirements/Stakeholders
    - What features are missing from current processors for HPC?
    - How does resilience/reliability factor in for SoCs?
    - Can a single SoC design capture what we need in HPC?
    - What are some key applications that would influence the SoC design?
- 14:00 – 16:00 EDA / IP
    - 14:00 – 14:20 Cadence (Chris Rowen)
    - 14:20 – 14:40 LBNL / OpenSoC (David Donofrio / Farzad Fatollahi-Fard)
    - 14:40 – 15:00 Break
    - 15:00 – 15:30 RISC--V (Krste Asanovic)
    - 15:30 – 15:50 Broadcom (Giri Chukkapalli)
- 16:00 – 17:00 Discussion Topic 2: Gap Analysis
    - What's missing to create an HPC SoC?
    - What are ways to address IP issues? (i.e. analog IP)
    - What IP do we need outside the SoC?
- 17:00 – 17:30 Wrap Up (John and Jim)