RISC-V Update

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Instruction Set Architectures don't matter

Most of the performance and energy running software on a computer is due to:

- Algorithms
- Application code
- Compiler
- OS/Runtimes
- ISA (Instruction Set Architecture)
- Microarchitecture (core + memory hierarchy)
- Circuit design
- Physical design
- Fabrication process

In an HPC *system*, there's also networks, storage, DC/DC converters, fans, …

ISAs do matter

- Most important interface in computer system
- Large cost to port and tune all ISA−dependent parts of a modern software stack
- Large cost to recompile/port/QA all supposedly ISA−independent parts of stack
- If using proprietary closed-source, don't have code
- If catch bit rot, no longer compile own source code
- Lost your own source code

- Most of the cost of developing a new chip is developing software for it

So…

If choice of ISA doesn't have much impact on system energy/performance, and it costs a lot to use different ones,

*why isn't there just **one free and open** industry-standard ISA?*

RISC-V Background

- In 2010, after many years and many projects using MIPS, SPARC, and x86 as basis of research, time to look at ISA for next set of projects
- Obvious choices: x86 and ARM
- x86 impossible – too complex, IP issues
  - 1300 instructions, x86 ISA manual 2900 pages, instruction length 1 to 15 bytes, ...
- ARM mostly impossible - baroque, IP issues
  -400 instructions, ARMv7 ISA manual 2700 pages
- So we started "3-month project" in summer 2010 to develop our own clean-slate ISA
- Four years later, we released frozen base user spec
  - But also many tape outs and several research publications

What's Different about RISC-V?

- *Simple*
  - Far smaller than other commercial ISAs
- *Clean-slate design*
  - Clear separation between user and privileged ISA
  - Avoids µarchitecture or technology-dependent features
- A *modular* ISA
  - Small standard base ISA
  - Multiple standard extensions
- Designed for *extensibility/specialization*
  - Variable-length instruction encoding
  - Vast opcode space available for instruction-set extensions
- *Stable*
  - Base and standard extensions are frozen
  - Additions via optional extensions, not new versions

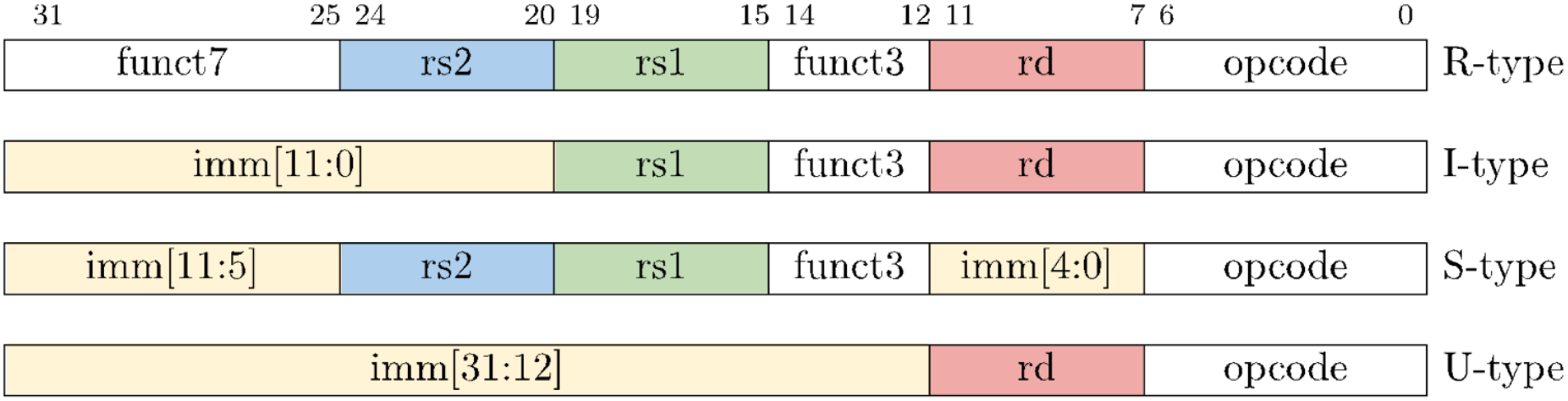
RISC-V is NOT an Open-Source Processor

- RISC-V is an ISA specification
- Want to encourage both open-source and proprietary implementations of the RISC-V ISA specification
- Most of cost of chip design is in software, so want to make sure software can be reused across many chip designs
- Expanding to specifications for whole platforms, including I/O and accelerators

RISC-V Base Plus Standard Extensions

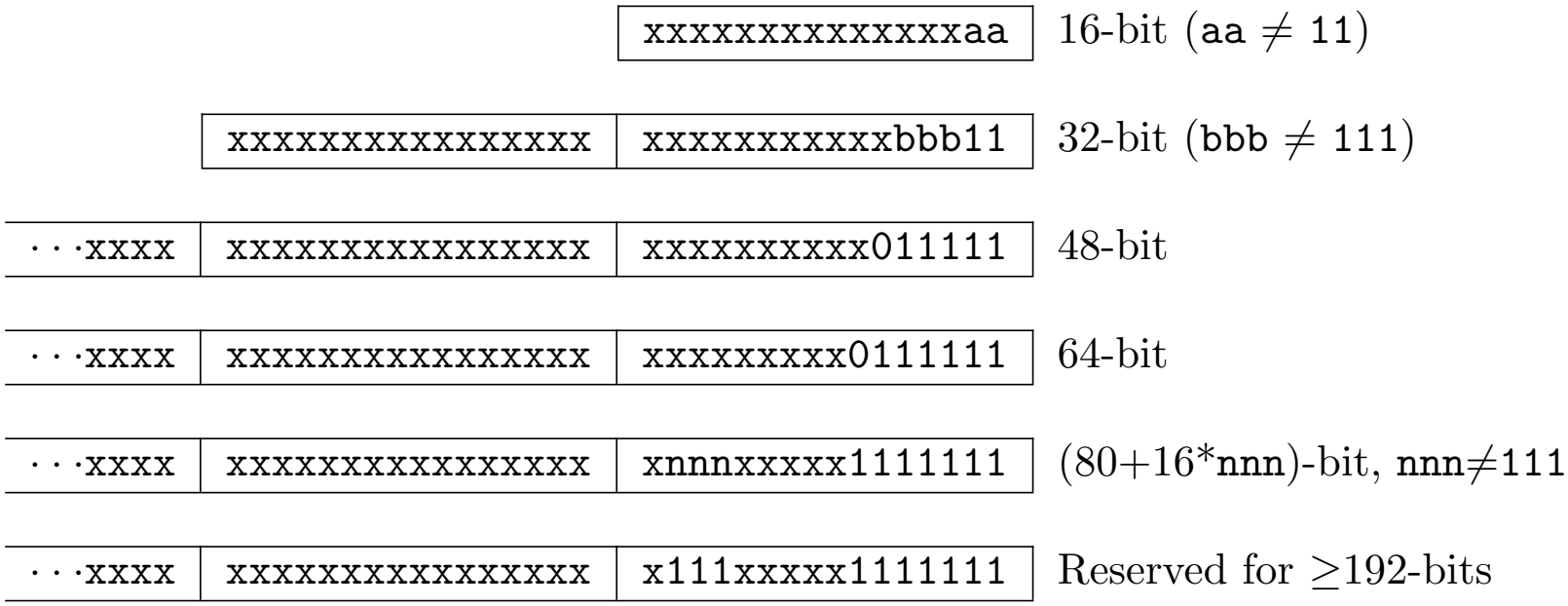
- ~~Three~~ Four base integer ISAs
  - RV32E, RV32I, RV64I, RV128I
  - RV32E is 16-register subset of RV32I
  - Only <50 hardware instructions needed
- Standard extensions
  - M: Integer multiply/divide
  - A: Atomic memory operations (AMOs + LR/SC)
  - F: Single-precision floating-point
  - D: Double-precision floating-point
  - G = IMAFD, "General-purpose" ISA
  - Q: Quad-precision floating-point
- All the above are a fairly standard RISC encoding in a fixed 32-bit instruction format
- Above user-level ISA components frozen in 2014
  - Supported forever after

RISC-V Standard Base ISA Details



- 32-bit fixed-width, naturally aligned instructions
- 31 integer registers x1-x31, plus x0 zero register
- rd/rs1/rs2 in fixed location, no implicit registers
- Immediate field (instr[31]) always sign-extended
- Floating-point adds f0-f31 registers plus FP CSR, also fused mul-add four-register format
- Designed to support PIC and dynamic linking

Variable-Length Encoding



- Extensions can use any multiple of 16 bits as instruction length
- Branches/Jumps target 16-bit boundaries even in fixed 32-bit base

"C": Compressed Instruction Extension

- Compressed code important for:
  - low-end embedded to save static code space
  - high-end commercial workloads to reduce cache footprint
- Standard extension (draft proposal released 5/28) adds 16-bit compressed instructions
  - 2-address forms with all 32 registers
  - 3-address forms with most frequent 8 registers
- Each **C** instruction expands to single base **I** instruction
- Original 32-bit instructions now can be 16-bit aligned
- Approximately 25-30% reduction in code size, with performance improvement from reduced I$ misses
- Surprisingly, lots of 16-bit encode space for future extensions

ARMv8 ISA vs. RISC-V ISA

Category	ARMv8	RISC-V	ARM/RISC
Year announced	2011	2011	--
Address sizes	32 / 64	32 / 64 / 128	--
Instruction sizes	32	16† / 32	--
Relative code size	1	0.75†	--
Instruction formats	53	6 / 12†	4X-8X
Data addressing modes	8	1	8X
Instructions	1070	177†	6X
Min number instructions to run Linux, gcc, LLVM	359	47	8X
Backend gcc compiler size	47K LOC	10K LOC	5X
Backend LLVM compiler size	22K LOC	10K LOC	2X
ISA manual size	5428 pages	163 pages	33X

MIPS manual 700 pages
80x86 manual 2900 pages

†With optional Compressed RISC-V ISA extension

RISC-V "Green Card"

RV32

RVI Base Instructions: RV32I

Category	Name	Fmt	RV32I Base	
Loads	Load Byte	I	LB	rd,rs1,imm
	Load Halfword	I	LH	rd,rs1,imm
	Load Word	I	LW	rd,rs1,imm
	Load Byte Unsigned	I	LBU	rd,rs1,imm
	Load Half Unsigned	I	LHU	rd,rs1,imm
Stores	Store Byte	S	SB	rs1,rs2,imm
	Store Halfword	S	SH	rs1,rs2,imm
	Store Word	S	SW	rs1,rs2,imm
Arithmetic	ADD	R	ADD	rd,rs1,rs2
	ADD Immediate	I	ADDI	rd,rs1,imm
	SUBtract	R	SUB	rd,rs1,rs2
	Load Upper Imm	U	LUI	rd,imm
	Add Upper Imm to PC	U	AUIPC	rd,imm
Shifts	Shift Left	R	SLL	rd,rs1,rs2
	Shift Left Immediate	I	SLLI	rd,rs1,shamt
	Shift Right	R	SRL	rd,rs1,rs2
	Shift Right Immediate	I	SRLI	rd,rs1,shamt
	Shift Right Arithmetic	R	SRA	rd,rs1,rs2
	Shift Right Arith Imm	I	SRAI	rd,rs1,shamt
Logical	XOR	R	XOR	rd,rs1,rs2
	XOR Immediate	I	XORI	rd,rs1,imm
	OR	R	OR	rd,rs1,rs2
	OR Immediate	I	ORI	rd,rs1,imm
	AND	R	AND	rd,rs1,rs2
	AND Immediate	I	ANDI	rd,rs1,imm
Compare	Set <	R	SLT	rd,rs1,rs2
	Set < Immediate	I	SLTI	rd,rs1,imm
	Set < Unsigned	R	SLTU	rd,rs1,rs2
	Set < Unsigned Imm	I	SLTIU	rd,rs1,imm
Branches	Branch =	SB	BEQ	rs1,rs2,imm
	Branch ≠	SB	BNE	rs1,rs2,imm
	Branch <	SB	BLT	rs1,rs2,imm
	Branch ≥	SB	BGE	rs1,rs2,imm
	Branch < Unsigned	SB	BLTU	rs1,rs2,imm
	Branch ≥ Unsigned	SB	BGEU	rs1,rs2,imm
Jump & Link	J&L	UJ	JAL	rd,imm
	Jump & Link Register	UJ	JALR	rd,rs1,imm
Synch	Synch threads	I	FENCE	
	Synch Instr & Data	I	FENCE.I	
System	System CALL	I	SCALL	
	System BREAK	I	SBREAK	
Counters	ReaD CYCLE	I	RDCYCLE	rd
	ReaD CYCLE upper Half	I	RDCYCLEH	rd
	ReaD TIME	I	RDTIME	rd
	ReaD TIME upper Half	I	RDTIMEH	rd
	ReaD INSTR RETired	I	RDINSTRET	rd
	ReaD INSTR upper Half	I	RDINSTRETH	rd

32-bit Formats

	31 27	26 25	24 20	19 15	14 12	11 7	6 0
R	funct7		rs2	rs1	funct3	rd	opcode
R4	rs3	funct2	rs2	rs1	funct3	rd	opcode
I	imm[11:0]			rs1	funct3	rd	opcode
S	imm[11:5]		rs2	rs1	funct3	imm[4:0]	opcode
SB	imm[12|10:5]		rs2	rs1	funct3	imm[4:1|11]	opcode
U	imm[31:12]					rd	opcode
UJ	imm[20|10:1|11|19:12]					rd	opcode

+ 12 for 64I

+ 8 for M

+ 4 for 64M

+ 11 for A

+ 11 for 64A

+ 31 for C

+ 34 for F, D, Q

+ 6 for 64F, 64D, 64Q

RISC-V "Green Card"

RV32I / RV64I / RV128I + C, M, A, F, D,& Q

RVI Base Instructions: RV32I, RV64I, and RV128I

Category	Name	Fmt	RV32I Base	+RV64	+RV128
Loads	Load Byte	I	LB rd,rs1,imm		
	Load Halfword	I	LH rd,rs1,imm		
	Load Word	I	LW rd,rs1,imm	LD rd,rs1,imm	LQ rd,rs2,imm
	Load Byte Unsigned	I	LBU rd,rs1,imm		
	Load Half Unsigned	I	LHU rd,rs1,imm	LWU rd,rs1,imm	LDU rd,rs1,imm
Stores	Store Byte	S	SB rs1,rs2,imm		
	Store Halfword	S	SH rs1,rs2,imm		
	Store Word	S	SW rs1,rs2,imm	SD rs1,rs2,imm	SQ rs1,rs2,imm
Arithmetic	ADD	R	ADD rd,rs1,rs2	ADDW rd,rs1,rs2	ADDD rd,rs1,rs2
	ADD Immediate	I	ADDI rd,rs1,imm	ADDIW rd,rs1,imm	ADDID rd,rs1,imm
	SUBtract	R	SUB rd,rs1,rs2	SUBW rd,rs1,rs2	SUBD rd,rs1,rs2
	Load Upper Imm	U	LUI rd,imm		
	Add Upper Imm to PC	U	AUIPC rd,imm		
Shifts	Shift Left	R	SLL rd,rs1,rs2	SLLW rd,rs1,rs2	SLLD rd,rs1,rs2
	Shift Left Immediate	I	SLLI rd,rs1,shamt	SLLIW rd,rs1,shamt	SLLID rd,rs1,shamt
	Shift Right	R	SRL rd,rs1,rs2	SRLW rd,rs1,rs2	SRLD rd,rs1,rs2
	Shift Right Immediate	I	SRLI rd,rs1,shamt	SRLIW rd,rs1,shamt	SRLID rd,rs1,shamt
	Shift Right Arithmetic	R	SRA rd,rs1,rs2	SRAW rd,rs1,rs2	SRAD rd,rs1,rs2
	Shift Right Arith Imm	I	SRAI rd,rs1,shamt	SRAIW rd,rs1,shamt	SRAID rd,rs1,shamt
Logical	XOR	R	XOR rd,rs1,rs2		
	XOR Immediate	I	XORI rd,rs1,imm		
	OR	R	OR rd,rs1,rs2		
	OR Immediate	I	ORI rd,rs1,imm		
	AND	R	AND rd,rs1,rs2		
	AND Immediate	I	ANDI rd,rs1,imm		
Compare	Set <	R	SLT rd,rs1,rs2		
	Set < Immediate	I	SLTI rd,rs1,imm		
	Set < Unsigned	R	SLTU rd,rs1,rs2		
	Set < Unsigned Imm	I	SLTIU rd,rs1,imm		
Branches	Branch =	SB	BEQ rs1,rs2,imm		
	Branch ≠	SB	BNE rs1,rs2,imm		
	Branch <	SB	BLT rs1,rs2,imm		
	Branch ≥	SB	BGE rs1,rs2,imm		
	Branch < Unsigned	SB	BLTU rs1,rs2,imm		
	Branch ≥ Unsigned	SB	BGEU rs1,rs2,imm		
Jump & Link	J&L	UJ	JAL rd,imm		
	Jump & Link Register	UJ	JALR rd,rs1,imm		
Synch	Synch threads	I	FENCE		
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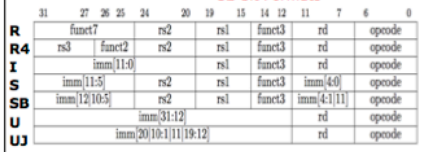
Counters	ReaD CYCLE	I	RDCYCLE rd		
	ReaD CYCLE upper Half	I	RDCYCLEH rd		
	ReaD TIME	I	RDTIME rd		
	ReaD TIME upper Half	I	RDTIMEH rd		
	ReaD INSTR RETired	I	RDINSTRET rd		
	ReaD INSTR upper Half	I	RDINSTRETH rd		

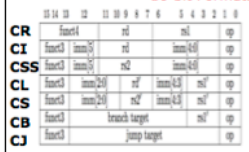
RVC Compressed Instruction Extension

Category	Name	Fmt	RVC	RVI equivalent
Loads	Load Word	CL	C.LW rd',rs1',imm	LW rd',rs1',imm*4
	Load Word SP	CI	C.LWSP rd,imm	LW rd,sp,imm*4
	Load Double	CL	C.LD rd',rs1',imm	LD rd',rs1',imm*8
	Load Double SP	CI	C.LDSP rd,imm	LD rd,sp,imm*8
	Load Quad	CL	C.LQ rd',rs1',imm	LQ rd',rs1',imm*16
	Load Quad SP	CI	C.LQSP rd,imm	LQ rd,sp,imm*16
Stores	Store Word	CS	C.SW rs1',rs2',imm	SW rs1',rs2',imm*4
	Store Word SP	CSS	C.SWSP rs2,imm	SW rs2,sp,imm*4
	Store Double	CS	C.SD rs1',rs2',imm	SD rs1',rs2',imm*8
	Store Double SP	CSS	C.SDSP rs2,imm	SD rs2,sp,imm*8
	Store Quad	CS	C.SQ rs1',rs2',imm	SQ rs1',rs2',imm*16
	Store Quad SP	CSS	C.SQSP rs2,imm	SQ rs2,sp,imm*16
Arithmetic	ADD	CR	C.ADD rd,rs1	ADD rd,rd,imm
	ADD Word	CR	C.ADDW rd,rs1	ADDW rd,rd,imm
	ADD Immediate	CI	C.ADDI rd,imm	ADDI rd,rd,imm
	ADD Word Imm	CI	C.ADDIW rd,imm	ADDIW rd,rd,imm
	ADD Imm * 4	CI	C.ADDI4 rd,imm	ADDI rd,rd,imm*4
	Load Immediate	CI	C.LI rd,imm	ADDI rd,x0,imm
	Load Upper Imm	CI	C.LUI rd,imm	LUI rd,imm
	MoVe	CR	C.MV rd,rs1	ADD rd,rs1,x0
Shifts	Shift Left Imm	CI	C.SLLI rd,imm	SLLI rd,rd,imm
Branches	Branch=0	CB	C.BEQZ rs1',imm	BEQ rs1,x0,imm
	Branch≠0	CB	C.BNEZ rs1',imm	BNE rs1,x0,imm
Jump & Link	J&L	CJ	C.J imm	JAL x0,imm
	Jump & Link Register	CR	C.JALR rd,rs1	JALR rd,rs1,0
System	Sys BREAK	CI	C.SBREAK	SBREAK

32-bit Formats



16-bit Formats



RVM Multiply-Divide Instruction Extension

Category	Name	Format	RV32M (Multiply-Divide)	+RV64	+RV128
Multiply	MULtiply	R	MUL rd,rs1,rs2	MULW rd,rs1,rs2	MULD rd,rs1,rs2
	MULtiply upper Half	R	MULH rd,rs1,rs2		
	MULtiply Half Sign/Uns	R	MULHSU rd,rs1,rs2		
	MULtiply upper Half Uns	R	MULHU rd,rs1,rs2		
Divide	DIVide	R	DIV rd,rs1,rs2	DIVW rd,rs1,rs2	DIVD rd,rs1,rs2
	DIVide Unsigned	R	DIVU rd,rs1,rs2		
Remainder	REMainder	R	REM rd,rs1,rs2	REMW rd,rs1,rs2	REMD rd,rs1,rs2
	REMainder Unsigned	R	REMU rd,rs1,rs2	REMUW rd,rs1,rs2	REMUD rd,rs1,rs2

RVA Atomic Instruction Extension

Category	Name	Format	RV32A (Atomic)	+RV64	+RV128
Load	Load Reserved	R	LR.W rd,rs1	LR.D rd,rs1	LR.Q rd,rs1
Store	Store Conditional	R	SC.W rd,rs1,rs2	SC.D rd,rs1,rs2	SC.Q rd,rs1,rs2
Swap	SWAP	R	AMOSWAP.W rd,rs1,rs2	AMOSWAP.D rd,rs1,rs2	AMOSWAP.Q rd,rs1,rs2
Add	ADD	R	AMOADD.W rd,rs1,rs2	AMOADD.D rd,rs1,rs2	AMOADD.Q rd,rs1,rs2
Logical	XOR	R	AMOXOR.W rd,rs1,rs2	AMOXOR.D rd,rs1,rs2	AMOXOR.Q rd,rs1,rs2
	AND	R	AMOAND.W rd,rs1,rs2	AMOAND.D rd,rs1,rs2	AMOAND.Q rd,rs1,rs2
	OR	R	AMOOR.W rd,rs1,rs2	AMOOR.D rd,rs1,rs2	AMOOR.Q rd,rs1,rs2
Min/Max	MINimum	R	AMOMIN.W rd,rs1,rs2	AMOMIN.D rd,rs1,rs2	AMOMIN.Q rd,rs1,rs2
	MAXimum	R	AMOMAX.W rd,rs1,rs2	AMOMAX.D rd,rs1,rs2	AMOMAX.Q rd,rs1,rs2
	MINimum Unsigned	R	AMOMINU.W rd,rs1,rs2	AMOMINU.D rd,rs1,rs2	AMOMINU.Q rd,rs1,rs2
	MAXimum Unsigned	R	AMOMAXU.W rd,rs1,rs2	AMOMAXU.D rd,rs1,rs2	AMOMAXU.Q rd,rs1,rs2

Three Floating-Point Instruction Extensions: RVF, RVD, & RVQ

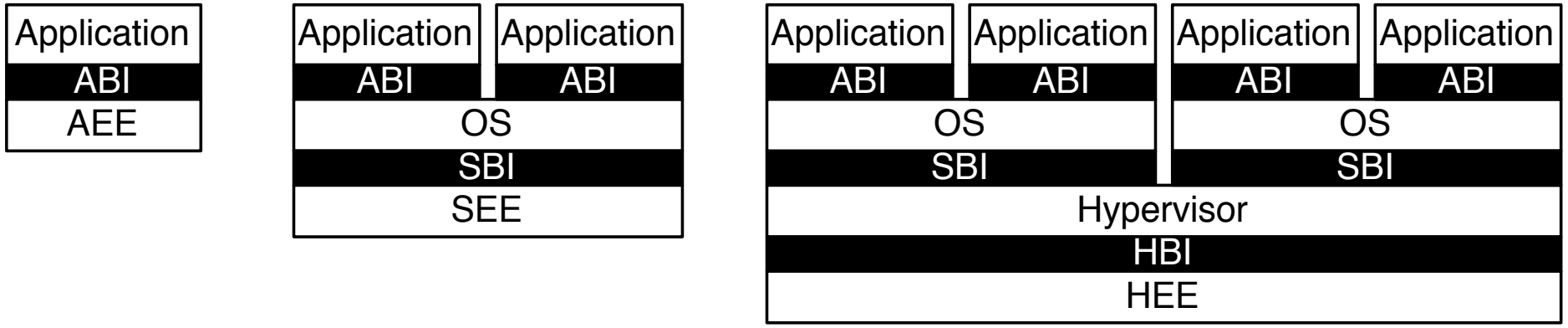
Category	Name	Format	RV32{F,D,Q} (SP,DP,QP Fl. Pt.)	+RV64	+RV128
Load	Load	I	FL{W,D,Q} rd,rs1,imm		
Store	Store	S	FS{W,D,Q} rs1,rs2,imm		
Arithmetic	ADD	R	FADD.{S,D,Q} rd,rs1,rs2		
	SUBtract	R	FSUB.{S,D,Q} rd,rs1,rs2		
	MULtiply	R	FMUL.{S,D,Q} rd,rs1,rs2		
	DIVide	R	FDIV.{S,D,Q} rd,rs1,rs2		
	SQuare RooT	R	FSQRT.{S,D,Q} rd,rs1		
Mul-Add	Multiply-ADD	R4	FMADD.{S,D,Q} rd,rs1,rs2,rs3		
	Multiply-SUBtract	R4	FMSUB.{S,D,Q} rd,rs1,rs2,rs3		
	Negative Multiply-SUBtract	R4	FNMSUB.{S,D,Q} rd,rs1,rs2,rs3		
	Negative Multiply-ADD	R4	FNMADD.{S,D,Q} rd,rs1,rs2,rs3		
Move	Move from Integer	R	FMV.S.X rd,rs1	FMV.D.X rd,rs1	FMV.Q.X rd,rs1
	Move to Integer	R	FMV.X.S rd,rs1	FMV.X.D rd,rs1	FMV.X.Q rd,rs1
Sign Inject	SiGN source	R	FSGNJ.{S,D,Q} rd,rs1,rs2		
	Negative SiGN source	R	FSGNJN.{S,D,Q} rd,rs1,rs2		
	Xor SiGN source	R	FSGNJX.{S,D,Q} rd,rs1,rs2		
Min/Max	MINimum	R	FMIN.{S,D,Q} rd,rs1,rs2		
	MAXimum	R	FMAX.{S,D,Q} rd,rs1,rs2		
Compare	Compare Float =	R	FEQ.{S,D,Q} rd,rs1,rs2		
	Compare Float <	R	FLT.{S,D,Q} rd,rs1,rs2		
	Compare Float ≤	R	FLE.{S,D,Q} rd,rs1,rs2		
Convert	Convert from Int	R	FCVT.{S,D,Q}.W rd,rs1	FCVT.{S,D,Q}.L rd,rs1	FCVT.{S,D,Q}.T rd,rs1
	Convert from Int Unsigned	R	FCVT.{S,D,Q}.WU rd,rs1	FCVT.{S,D,Q}.LU rd,rs1	FCVT.{S,D,Q}.TU rd,rs1
	Convert to Int	R	FCVT.W.{S,D,Q} rd,rs1	FCVT.L.{S,D,Q} rd,rs1	FCVT.T.{S,D,Q} rd,rs1
	Convert to Int Unsigned	R	FCVT.WU.{S,D,Q} rd,rs1	FCVT.LU.{S,D,Q} rd,rs1	FCVT.TU.{S,D,Q} rd,rs1
Categorization	Classify Type	R	FCLASS.{S,D,Q} rd,rs1		
Configuration	Read Status	R	FRCSR rd		
	Read Rounding Mode	R	FRRM rd		
	Read Flags	R	FRFLAGS rd		
	Swap Status Reg	R	FSCSR rd,rs1		
	Swap Rounding Mode	R	FSRM rd,rs1		
	Swap Flags	R	FSFLAGS rd,rs1		
	Swap Rounding Mode Imm	I	FSRMI rd,imm		
	Swap Flags Imm	I	FSFLAGSI rd,imm		

Upcoming Vector Extension

- Traditional vector extension
  - similar to Cray-style vector ISA, not packed-SIMD ISA
- LLVM-based compiler support for two programming models:
  - Auto-vectorization/parallelization (OpenMP)
  - Explicit SPMD (OpenCL)

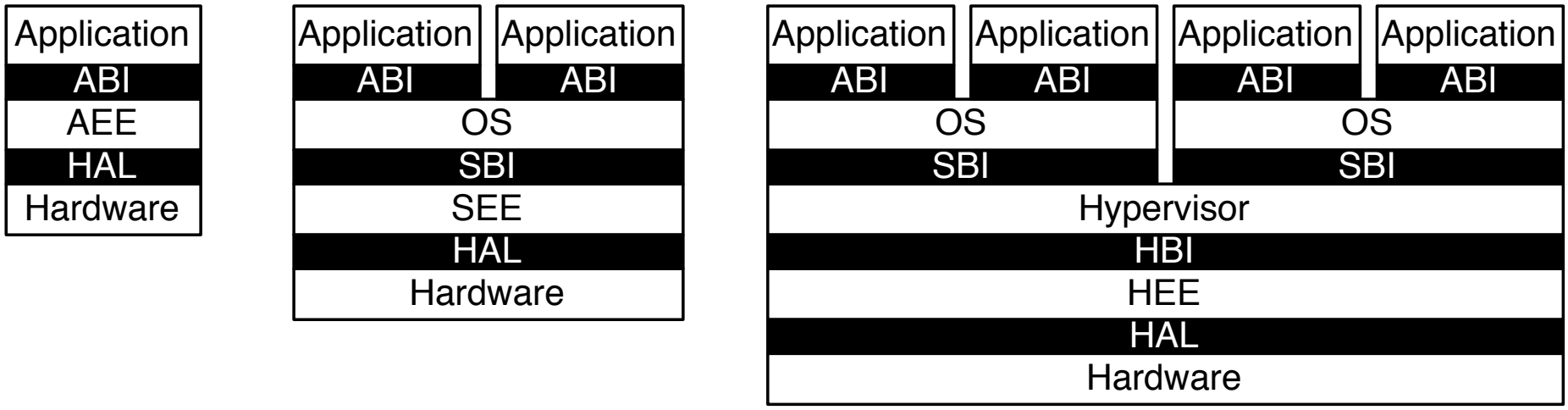
- In progress, to be released in near future for comments

RISC-V Privileged Architecture



- Provide clean split between layers of the software stack
- Application communicates with Application Execution Environment (AEE) via Application Binary Interface (ABI)
- OS communicates via Supervisor Execution Environment (SEE) via System Binary Interface (SBI)
- Hypervisor communicates via Hypervisor Binary Interface to Hypervisor Execution Environment
- All levels of ISA designed to support virtualization

RISC-V Hardware Abstraction Layer



- Execution environments communicate with hardware platforms via Hardware Abstraction Layer (HAL)
- Details of execution environment and hardware platforms isolated from OS/Hypervisor ports

RISC-V Privileged Architecture

- Draft specification released for comments 5/9/2015
- Four privilege modes
  - User (U-mode)
  - Supervisor (S-mode)
  - Hypervisor (H-mode) // Not specified yet
  - Machine (M-mode)
- Supported combinations of modes:
  - M (simple embedded systems)
  - M, U (embedded systems with protection)
  - M, S, U (systems running Unix-style operating systems)
  - M, H, S, U (systems running Hypervisors)

Small System Memory-Management Architectures

- Mbare
  - Bare metal, no translation or protection
- Mbb
  - Base-and-bounds protection

- Mbare is also the memory-management mode the machine enters at reset

Virtual Memory Architectures

- Designed to support current Unix-style operating systems
- Sv32
  - Demand-paged 32-bit virtual address spaces
- Sv39
  - Demand-paged 39-bit virtual address spaces
- Sv48
  - Demand-paged 48-bit virtual address spaces

- 4KiB pages, 2MiB Megapages, 1GiB Gigapages
  - 4KiB base page size to keep software developers happy, reduce internal fragmentation
  - Rely on better TLB hierarchy to support 4KiB pages well

RISC-V Ecosystem

www.riscv.org

- ***Documentation***
  - User-Level ISA Spec v2
  - Privileged ISA draft
  - Compressed ISA draft
- ***Software Tools***
  - GCC/glibc/GDB
  - LLVM/Clang
  - Linux
  - Yocto
  - Verification Suite
- ***Hardware Tools***
  - Zynq FPGA Infrastructure
  - Chisel
- ***Software Implementations***
  - ANGEL, JavaScript ISA Sim.
  - Spike, In-house ISA Sim.
  - QEMU
- ***Hardware Implementations***
  - Rocket Chip Generator
    - RV64G single-issue in-order pipe
  - Sodor Processor Collection
  - External implementations

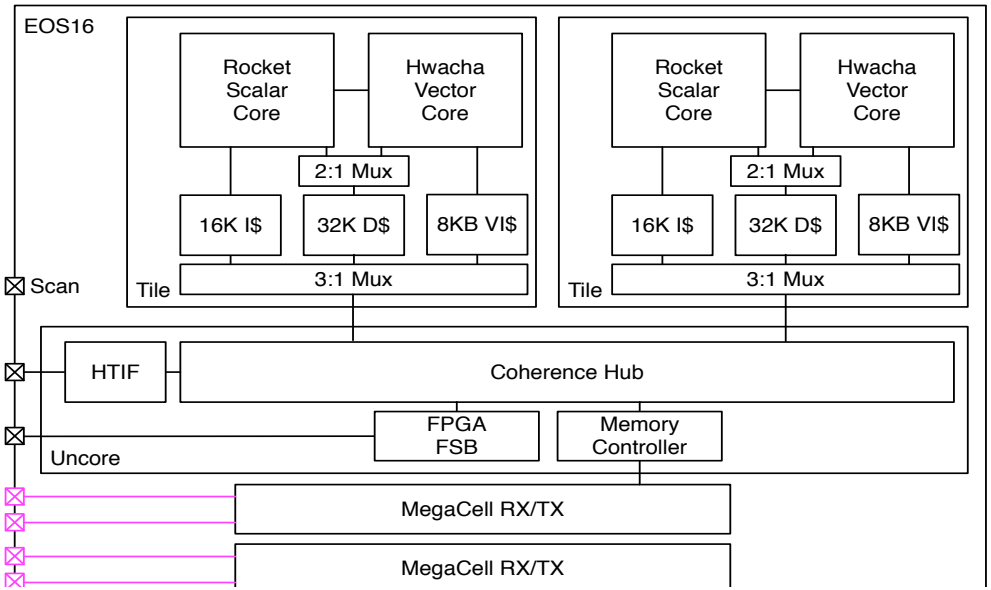
"Rocket Chip" Generator Alpha Release, Oct 7, 2014

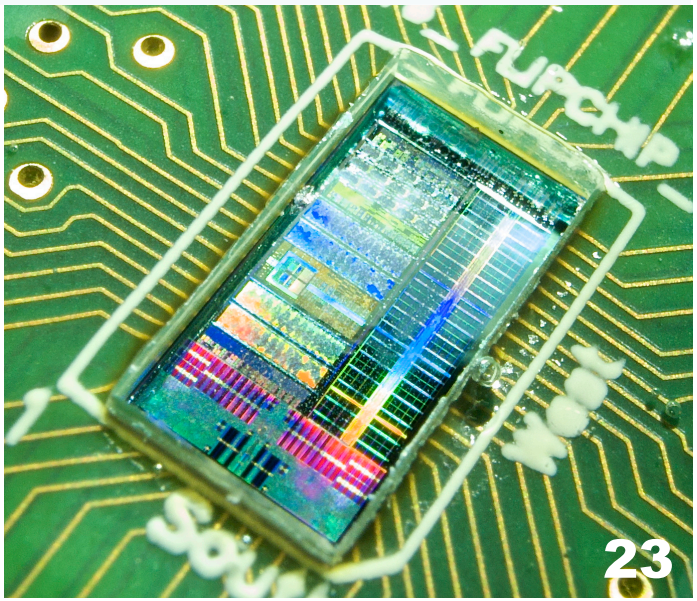
- Single-issue in-order classic 5-stage RISC pipeline
- Fully pipelined IEEE-2008 32-bit/64-bit FPU
- MMU supports Linux, other OS
- Non-blocking data cache
- BTB, BHT, RAS branch prediction
- Coprocessor interface
- Similar design point to ARM A5
- Parameterized generator written in Chisel
- ~5,400 LOC in for processor
- ~2,000 LOC for floating-point core
- ~4,600 LOC for "uncore" (coherence hubs, L2 caches, networks, host/target interfaces)

EOS Chip Roadmap in IBM 45nm SOI

(design/fabrication funded by DARPA PERFECT/POEM)

Chip	Tapeout	Receipt	DP GF/W	Notes
EOS14	Mar'12	Sep'12	5.0	"ESP-0" Rocket + Hwacha vector unit. First "Chisel"-ed RISC-V core.
EOS16	Aug'12	Mar'13	—	Dual-core cache-coherent Rocket + Hwacha. Broken pad drivers, IBM's bug.
EOS18	Feb'13	Jul'13	16.7	Dual-core cache-coherent Rocket + Hwacha. QoR improvements: dual VT flow; hierarchical P&R; RTL improvements for dynamic power & clock rate
EOS20	Jul'13	Jan'14	14.1	Dual-core design from ESP-1 chip generator. Multi-VT flow. Runs Linux. Raven-3 from same RTL.
EOS22	Mar'14	Sep'14		EOS20 + bug fixes + faster FPU
EOS24	Mar'15	??		Initial version of ESP-2; FireBox chip prototype



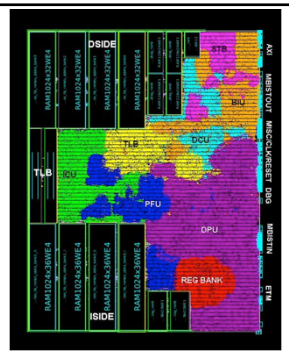


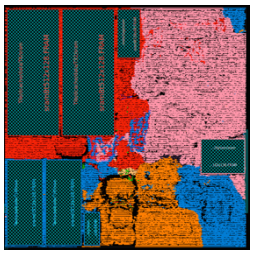
ARM Cortex A5 vs. RISC-V Rocket

Category	ARM Cortex A5	RISC-V Rocket
ISA	32-bit ARM v7	64-bit RISC-V v2
Architecture	Single-Issue In-Order 8-stage	Single-Issue In-Order 5-stage
Performance	1.57 DMIPS/MHz	1.72 DMIPS/MHz
Process	TSMC 40GPLUS	TSMC 40GPLUS
Area w/o Caches	0.27 mm^2	0.14 mm^2
Area with 16K Caches	0.53 mm^2	0.39 mm^2
Area Efficiency	2.96 DMIPS/MHz/mm^2	4.41 DMIPS/MHz/mm^2
Frequency	>1GHz	>1GHz
Dynamic Power	<0.080 mW/MHz	0.034 mW/MHz

Rocket Area Numbers Assuming 85% Utilization, the same number ARM used to report area.

Plots are not to scale.





Zscale Core Generator

- Tiniest RISC-V so far: RV32IM
- Single-issue in-order 3-stage RISC pipeline
- Similar design point to ARM M0
  - But has 32 registers, Multiply/Divide unit, performance counters, privileged mode
- Parameterized generator in Chisel + Verilog version
  - 538 unique LOC in Chisel for processor
  - 983 LOC in Chisel borrowed from Rocket
- TSMC40G, assuming 85% utilization factor for PNR

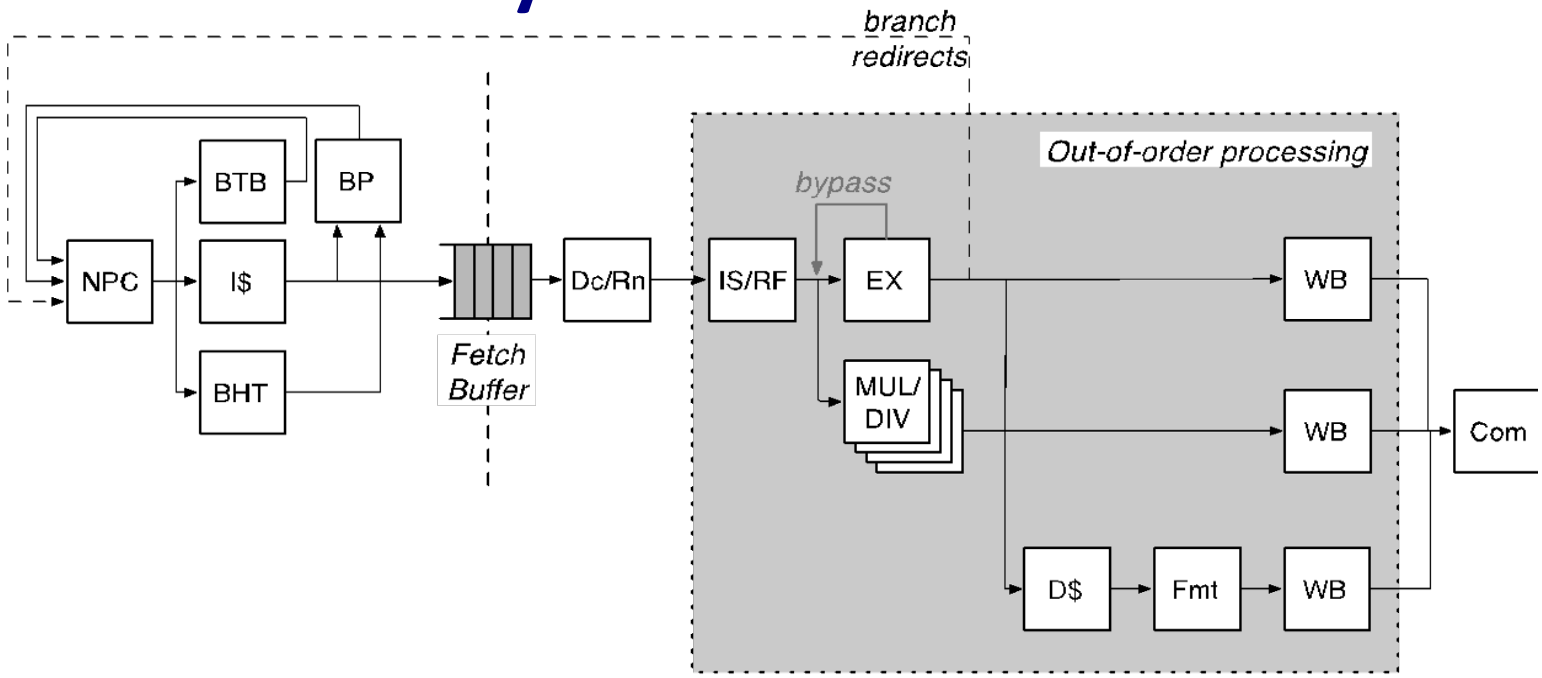
Clock Rate (MHz)	*DMIPS/ MHz*	*Area (mm^2)*	*Power (μW)*	*Power Efficiency (μW/MHz)*	*DMIPS/ MHz/mm^2*
500	1.35	0.0120	822	1.6	112
100	1.35	0.0098	181	1.8	138

ARM Cortex M0 vs. RISC-V Zscale

Category	ARM Cortex M0	RISC-V Zscale
ISA	32-bit ARM v6	32-bit RISC-V (RV32IM)
Architecture	Single-Issue In-Order 3-stage	Single-Issue In-Order 3-stage
Performance	0.87 DMIPS/MHz	1.35 DMIPS/MHz
Process	TSMC 40GPLUS	TSMC 40GPLUS
Area w/o Caches	0.0070 mm^2	0.0098 mm^2
Area Efficiency	124 DMIPS/MHz/mm^2	138 DMIPS/MHz/mm^2
Frequency	≤50 MHz	100 MHz
Voltage (RTV)	1.1 V	0.99 V
Dynamic Power	5.1 µW/MHz	1.8 µW/MHz

ARM: area, power 40LP process, minimum configuration; DMIPS with multiply support
http://www.arm.com/products/processors/cortex-m/cortex-m0

BOOM: Berkeley Out-of-Order Machine

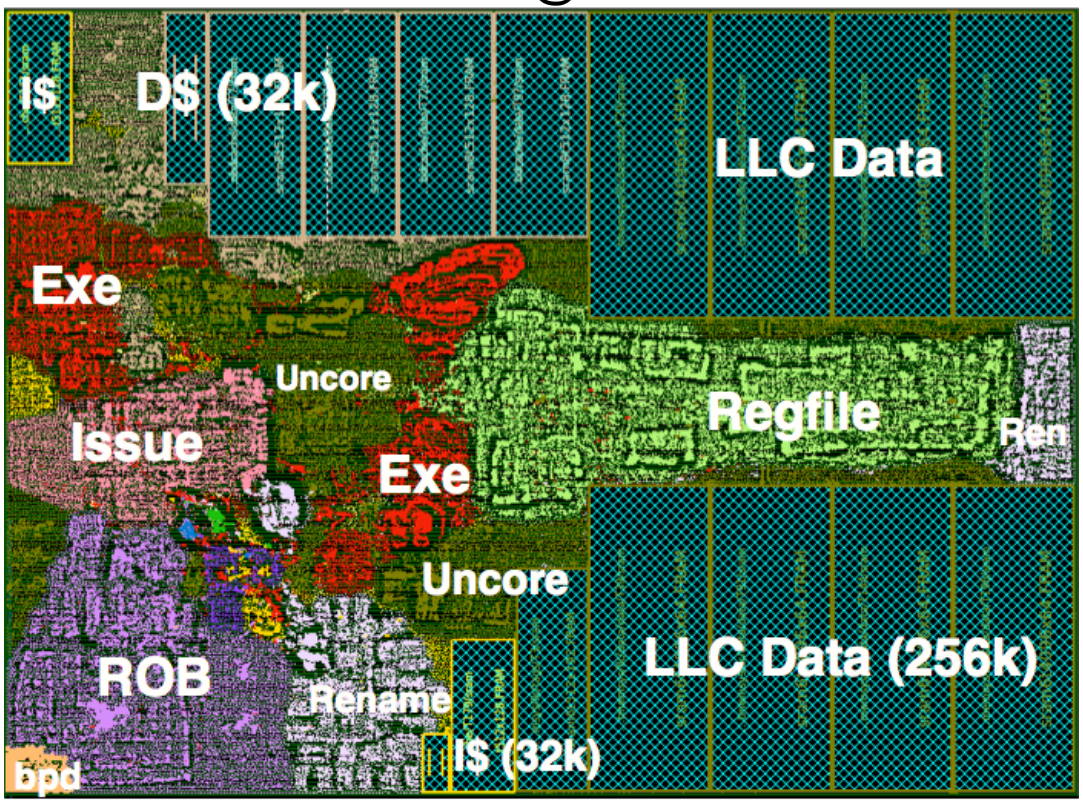


- ~9,000 LOC in BOOM github repo
- additional ~11,500 loc instantiated from other libraries
  - ~5,000 LOC from Rocket core repository
    - functional units, caches, PTWs, etc.
  - ~4,500 LOC from uncore
    - coherence hubs, L2 caches, networks, host/target interfaces
  - ~2000 LOC from hardfloat
    - floating-point hardware units

Synthesizable

- Runs on FPGA
  - (Zynq zedboard and Zynq zc706)
- 2GHz (30 FO4) in TSMC 45nm
  - speed of logic (SRAM is slower)

1.7mm2 @ 45nm



2-wide BOOM layout.

Comparison against ARM A9

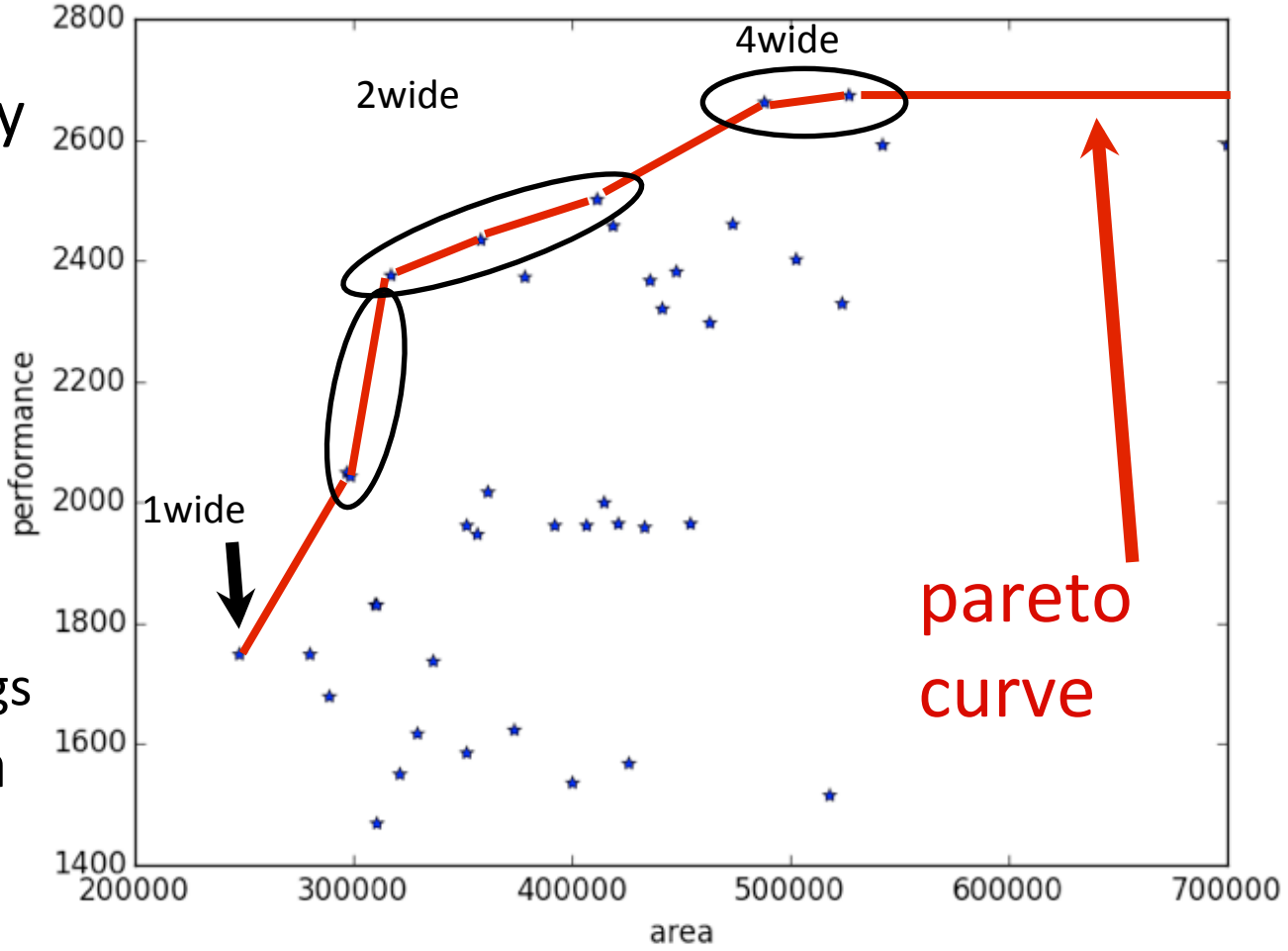
Category	ARM Cortex-A9	RISC-V BOOM-2w
ISA	32-bit ARM v7	64-bit RISC-V v2 (RV64G)
Architecture	2 wide, 3+1 issue Out-of-Order 8-stage	2 wide, 3 issue Out-of-Order 6-stage
Performance	3.59 CoreMarks/MHz	3.91 CoreMarks/MHz
Process	TSMC 40GPLUS	TSMC 40GPLUS
Area with 32K caches	2.5 mm^2	1.00 mm^2
Area efficiency	1.4 CoreMarks/MHz/mm^2	3.9 CoreMarks/MHz/mm^2
Frequency	1.4 GHz	1.5 GHz

Caveats: A9 includes NEON
BOOM is 64-bit, has IEEE-2008 fused mul-add

Design-space exploration

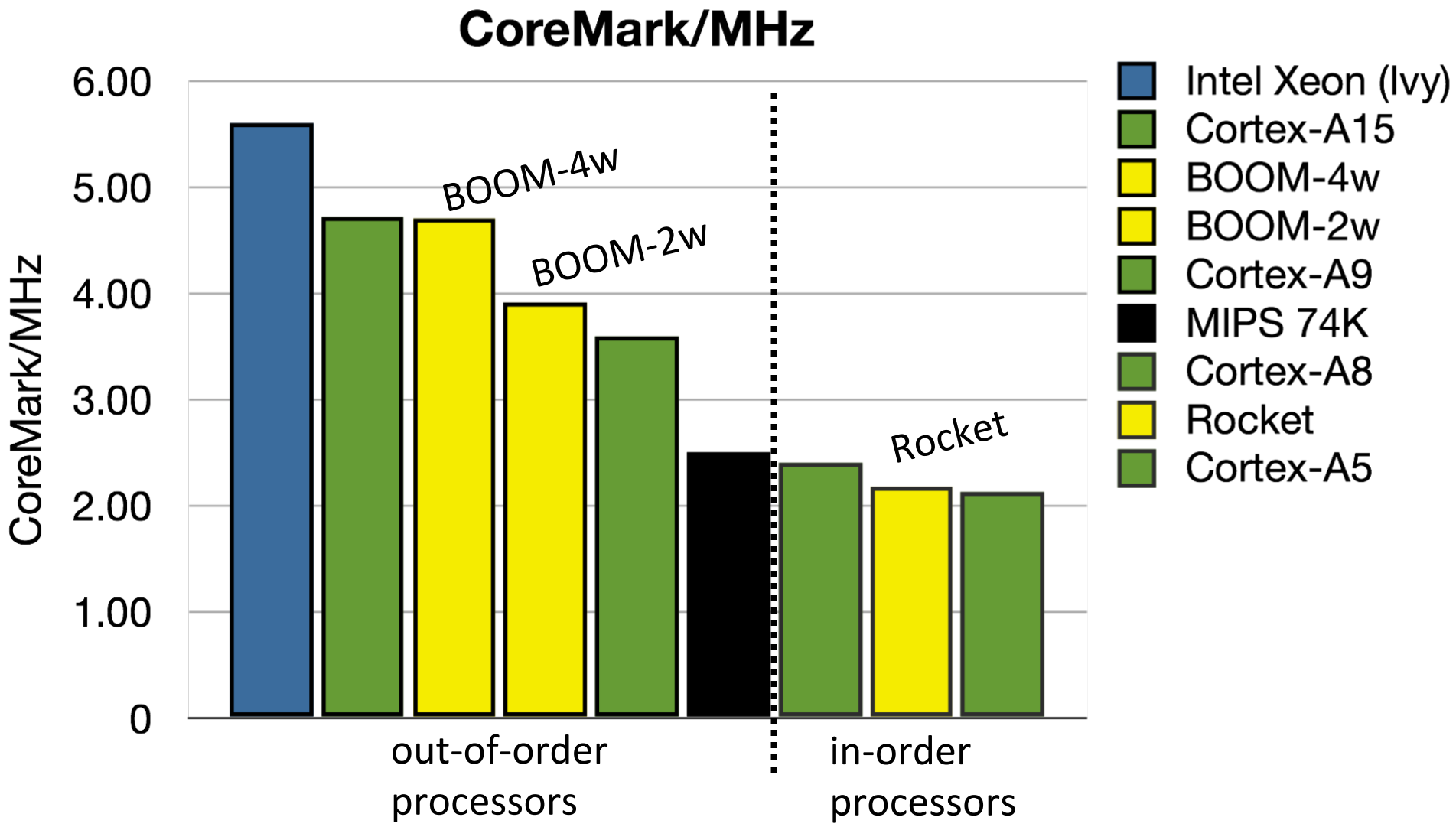
- Very preliminary
- Parameters
  - fetch width
  - issue width
  - ROB size
  - IW size
  - LSU size
  - Regfile size
  - # of branch tags
- 3x range in area
- 2x range in performance

Perf (CoreMark/s) vs. Area (um^2)



data collected by Orianna DeMasi

Industry Comparisons



RISC-V Outside Berkeley

- Adopted as “standard ISA” for **India**. IIT-Madras building 6 different open-source cores, from microcontrollers to servers
- **Bluespec** Inc. developing RISC-V cores for use in tightly integrated hardware/software IP blocks
- **LowRISC** project based in Cambridge, UK producing open-source RISC-V Rocket-based SoCs. Led by one of the founders of Raspberry Pi, and privately funded
- First commercial RISC-V cores have already shipped!
- Multiple commercial silicon implementations for sale later this year

Learning More about RISC-V

- Sign up for mailing lists/twitter at **`riscv.org`** to get announcements
- 1st RISC-V workshop was January 14 - 15 in Monterey
  - Slides & videos: riscv.org/workshop-jan2015.html
  - Sold out: 144 attendees from 33 companies and 14 universities
- 2nd RISC-V workshop June 29 - 30 at UC Berkeley
  - Free to academics and ASPIRE lab sponsors; $149 for others
    - Will likely sell out too, so sign up soon
  - Agenda: http://riscv.org/workshop-jun2015.html
  - Sign up: www.regonline.com/riscvworkshop2

RISC-V Foundation

- Mission statement

  "*to standardize, protect, and promote the free and open RISC-V instruction set architecture and its hardware and software ecosystem for use in all computing devices*."

- Establishing a 501(c)(6) foundation
- Rick O'Connor recruited as Executive Director
- Currently recruiting "founding" member companies

RISC-V Landscape

RISC-V Foundation (US non-profit)
In process

Govt/Public Open Source	Non-Profit Private Ventures	Commercial Providers
UC Berkeley (Originators, developers)	lowRISC (UK non-profit)	Bluespec
IIT Madras (Indian Govt.)		Rumble
		TenX
		Startup-X???
		Startup-Y???

Modest RISC-V Project Goal

Become the industry-standard ISA for all computing devices