Exceptional service in the national interest

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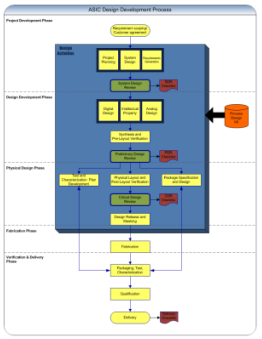

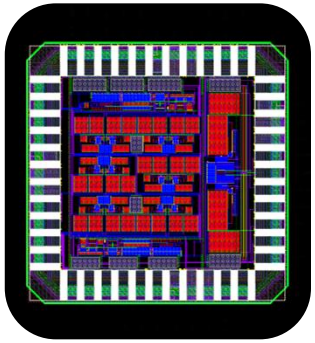

State-of-Art (SoA) System-on-Chip (SoC) Design
HPC SoC Workshop

Michael Holmes

Manager, Mixed Signal ASIC/SoC Products

Sandia National Laboratories

505-284-9673

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U.S. DEPARTMENT OF ENERGY | National Nuclear Security Administration

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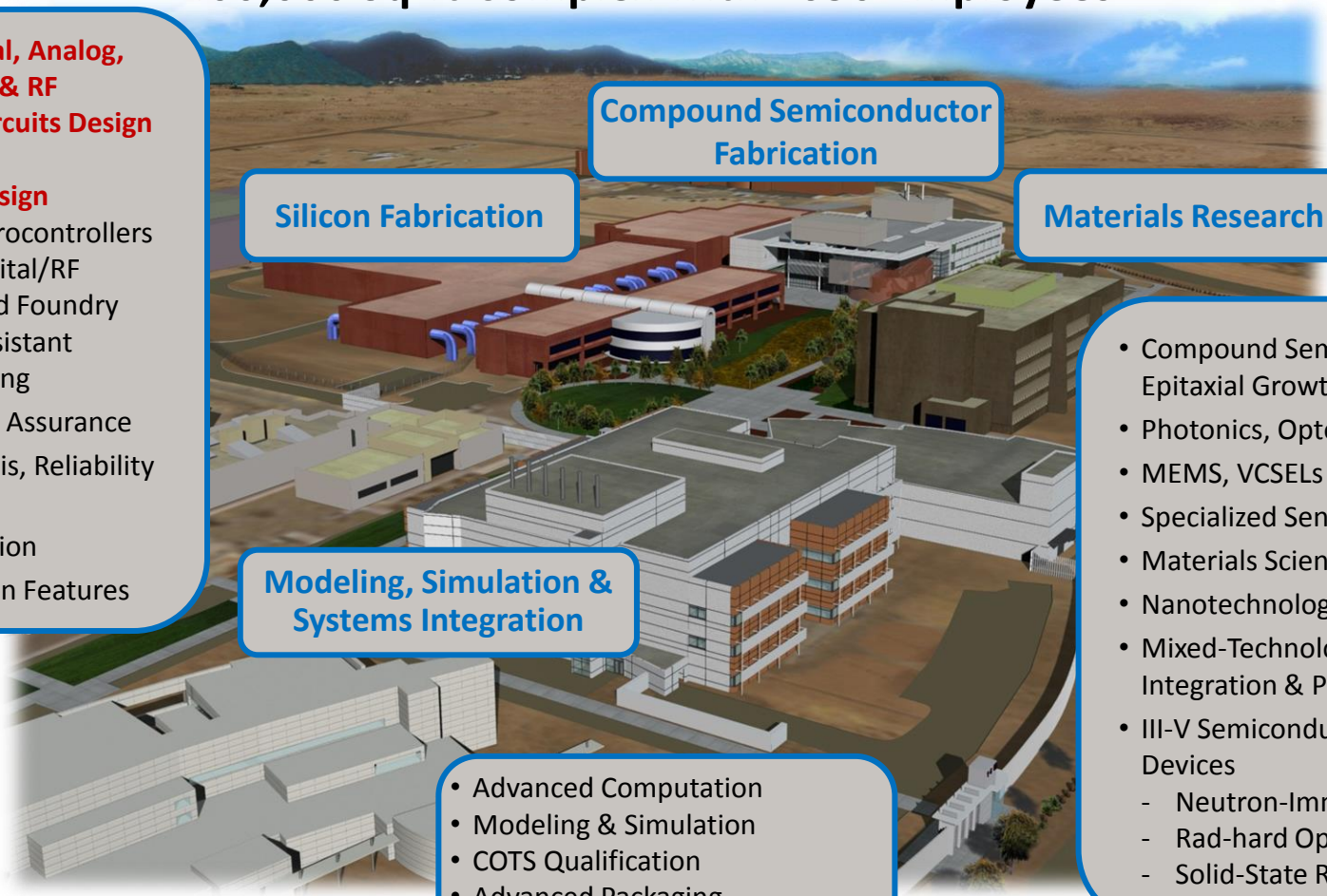
Sandia Microsystems & Engineering Sciences Applications (MESA)

Sandia National Laboratories

400,000 Sq-ft Complex with >650 Employees

- **Trusted Digital, Analog, Mixed Signal & RF Integrated Circuits Design** & Fabrication
- **Custom IC Design**
  - Secure microcontrollers
  - Analog/Digital/RF
  - IBM Trusted Foundry
  - Tamper Resistant
- Micromachining
- RAD Effects & Assurance
- Failure Analysis, Reliability Physics
- Test & Validation
- 3-D Integration Features



- Compound Semiconductor Epitaxial Growth
- Photonics, Optoelectronics
- MEMS, VCSELs
- Specialized Sensors
- Materials Science
- Nanotechnology, Chem/Bio
- Mixed-Technology Integration & Processing
- III-V Semiconductor Devices
  - Neutron-Immune HBT
  - Rad-hard Optical Links
  - Solid-State RF Devices

- Advanced Computation
- Modeling & Simulation
- COTS Qualification
- Advanced Packaging
- Custom Electronic Components
- System Design & Test

Mixed Signal ASIC/SoC

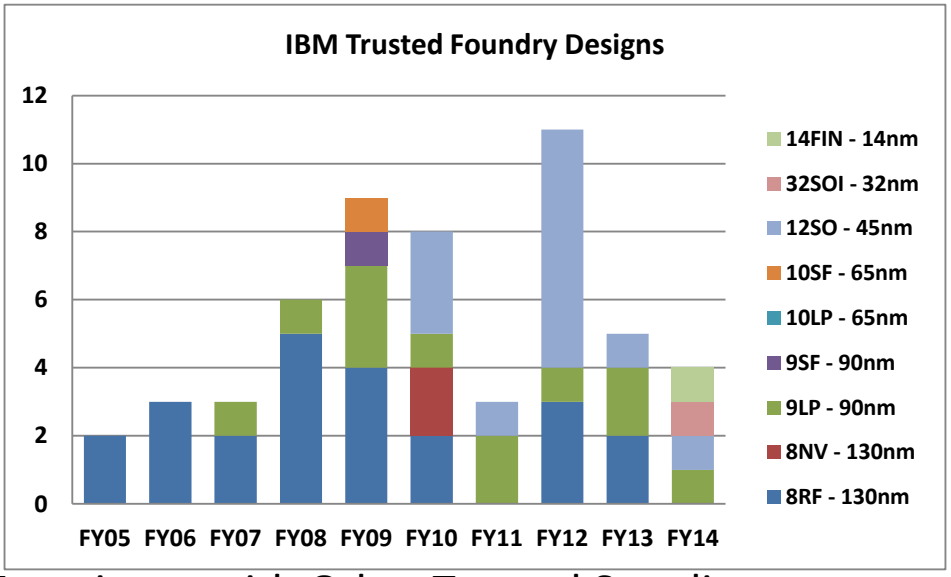
Sandia Microelectronics Development

- Develop *digital, analog, and mixed-signal integrated circuits (IC)* along with a deep understanding of technology offerings and design methodologies
- Develop *trusted* integrated circuits
  - Access to trusted resources and facilities for design, layout, fabrication, packaging, test, qualification, and product delivery assuring full chain-of-custody
    - On-shore, US owned
    - Security clearances, processes and/or facilities
    - DOD trusted accreditation
  - Mature relationship with IBM Trusted foundry using advanced technology
  - Access to other government trusted suppliers
- Develop *radiation hardened* integrated circuits
  - Access to strategic radiation hardened in-house technology
  - Radiation hardened by design for commercial technologies
- Develop *high-reliability* integrated circuits for *high consequence systems*
  - Weapons system components
  - Security-based and/or classified components
- Deliver *low volume* integrated circuits
  - Providing ICs where commercial industry cannot or will not supply

Mixed Signal ASIC/SoC

Sandia Trusted Design

- Delivering ASICs from Sandia Radiation Hardened Trusted Foundry
  - Meets the needs for strategic radiation hardened programs
  - Flexible to accommodate research activities
- IBM Trusted Foundry: 52 Designs

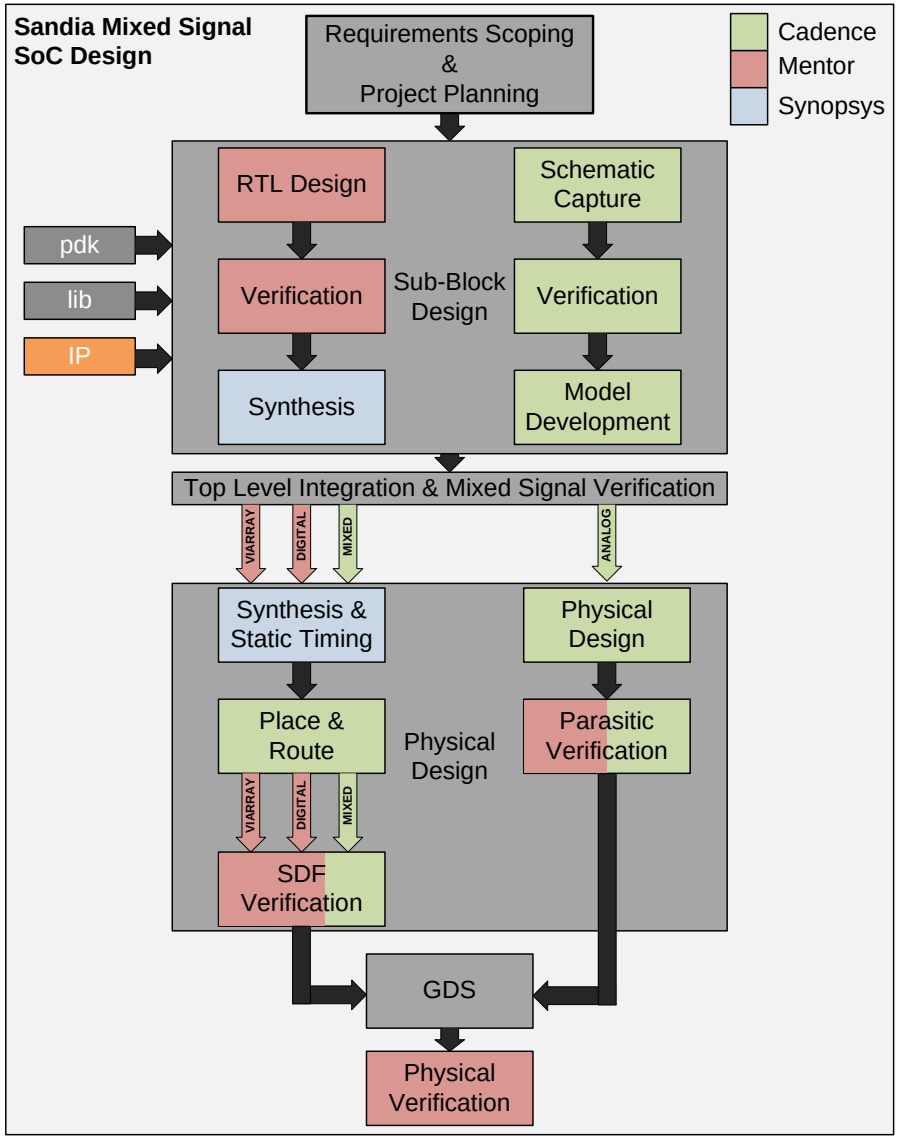


- History and Experience with Other Trusted Suppliers
  - National Semiconductor Corporation Foundry
  - Honeywell Foundry
  - Partnerships with Northrop Grumman
  - Jazz Semiconductor

Mixed Signal ASIC/SoC

Sandia Mixed Signal SoC Design

- Full Mixed-Signal IC Design Flow
  - Industry Standard EDA/CAD Tools
  - Mixed-Signal Verification & Co-Simulation
    - SPICE; Verilog-A; AMS; RTL
- SoA SoC Verification
  - Universal Verification (UVM)
  - Formal Verification
- SoA Synthesis & APR Flow
- Intellectual Property (IP)
  - Silicon Fabric/Motherboard SoC Design
  - Integration & Verification
  - Custom IP (Hard & Soft)
- 3D Integration & Verification Flow
  - 3D Automated Place & Route
  - 3D Verification



Mixed Signal ASIC/SoC

SoC Design Abstraction Evolution & HPC

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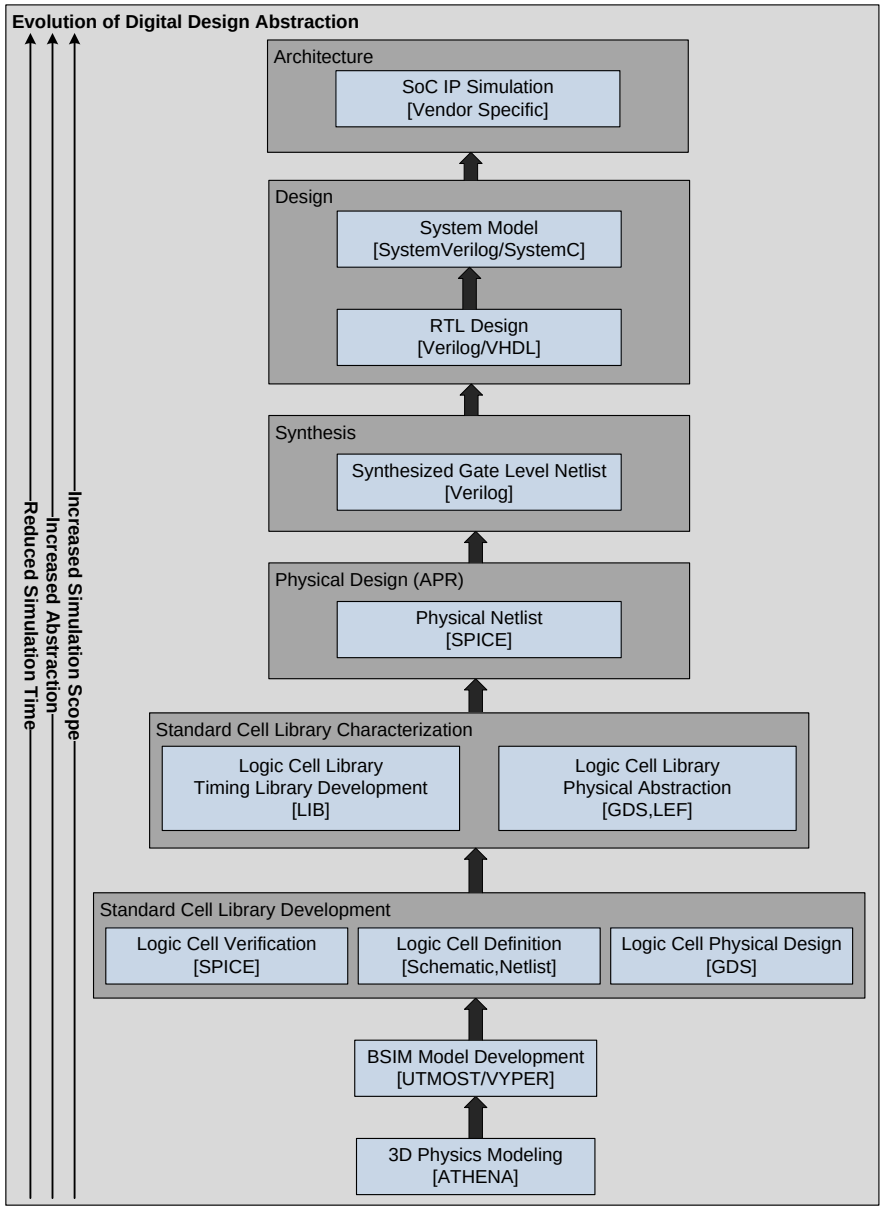
- Evolution of abstraction (Digital/Analog/AMS)
  - Driven by complexity, cost, & time to market
  - Analogous to the evolution of COTs PCB design
  - Chip scale architecture evaluation & trade space
  - Rapidly optimize architecture to the problem
- New hierarchy of designers in SoC development
  - System level designers drive architecture trades
  - Rapid prototyping & simulation tools
  - High performance, scalable, multi-core platforms
- Proliferation of suite of IP building blocks
  - Silicon fabric or motherboard (3D?)
  - Reduced cost and risk
    - Pre-verified IP with design kits
    - Verification suite
    - Optimized for yield and manufacturing
- FPGA SoC platforms
  - Traditional FPGA benefits
  - Less flexibility



Mixed Signal ASIC/SoC

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3D Integration Development & Commercial Adoption

- Niche applications with specialized process flows
- Requires specialized processing, tools, materials research
- Additional yield loss in handling and process steps
- New design and test paradigms
  - Limited CAD tool support (custom flow development)
  - Combined assembly & test for yield (known good die)
- Limited by additional cost of 2.5D/3D fabrication
  - Through Silicon Via's (TSV)
    - Precision Etch & Singulation
    - Liner Deposition & Metal Fill
  - Bonding
  - TSV Exposure
    - Backgrinding and Thinning

Commercial Trends

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- 2.5D will continue to see extended use and will dominate market first
  - Easy adoption (evolutionary not revolutionary)
- 3D Drivers
  - High performance processors to overcome bandwidth limitations and improve power performance
  - Mixed-signal designs in which analog functionality does not benefit from node shrink (cost savings)
  - Higher cost of adoption, requires new paradigm in design
  - Heterogeneous integration may offset cost of adoption long-term
- Applications drive development
  - High Density Interconnect:
    - Pixelated sensors require high density interconnect, small pitch, millions of connections
    - Can tolerate less than 100% functionality (a dead pixel is “ok”)
  - Low/Medium Density Interconnects:
    - High performance processors and custom heterogeneous solutions will drive low/medium density solutions.
    - Requires high yield and will tolerate larger interconnects.

3D Integration Considerations
Custom u-Systems & Heterogeneous Integration

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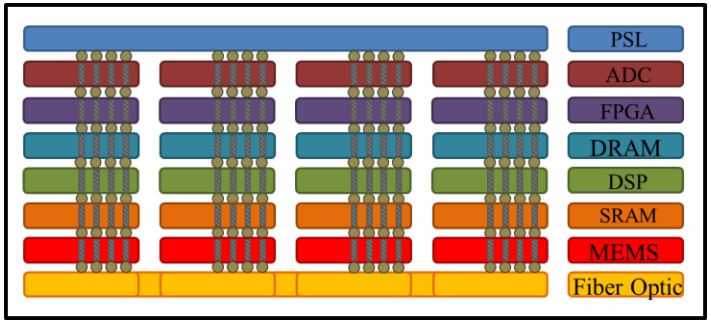

- Layer-to-Layer Interconnect Density
- TSV Requirements (diameter, pitch)
- Stacked Alignment Accuracy
- Tiling Accuracy Placement Requirements
- Wafer Level vs. Die Level Requirements & Assembly
  - Most High Density Processes Require Wafer-To-Wafer Bonding
    - Wafer level processing required to define TSV's and interconnect layers
    - Wafer level processing required to thin wafer backside to reveal TSV's
  - Wafer Level Fabrication At Advanced Technology Nodes Can Be Cost Prohibitive
  - Costs Are More Manageable Using Multi-Project Wafer (MPW) Runs
    - Wafer contains designs for other users; Only die are ultimately available, which can complicate 3D processing approach
    - Circuitry must be partitioned to contain interconnect density

Mixed Signal ASIC/SoC